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A novel three-phase buck-boost inverter controlled by an open-loop assisted closed-loop hybrid control method

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Summary

A novel general purpose three-phase buck-boost inverter without need of additional filtering units is presented in this study. The proposed inverter topology is built with moderate numbers of elements in terms of the operation advantages and qualities. The buck-boost converter-based structure provides obtaining wide-range output voltage amplitudes lower or higher than the input voltages. A novel hybrid control method that is open-loop assisted closed-loop control is proposed for the inverter operation to improve the response performance on various input and output operation conditions. The wye-connected modular structure of the proposed inverter topology also enables unbalanced three-phase operation and single-phase operation for each phase with independent phase voltages and frequencies. An experimental laboratory setup is built for the proposed three-phase inverter for 0–50 Hz, 0–100 Vp, and 1.5 kW operation values for real-time application tests. Simulation tests are also applied for the inverter. The obtained results for both the simulation and the experimental tests show that the presented inverter with the proposed hybrid control method is capable of operating in balanced/unbalanced three-phase and independent single-phase modes while producing close to sine wave output voltages under 5% THD levels with wide range desired amplitudes and frequencies on different operating points.

KEYWORDS

buck-boost converter, harmonics, inverter, THD, three-phase

1 | INTRODUCTION

Three-phase inverters find wide area in the application, so there are many studies of three-phase inverters in the literature.[1–3] The studies focus on developing new topologies that aim to produce high-quality phase voltages also providing less density, cost, and complexity.[4] According to the IEEE standards, alternating current (AC) customers have to be supplied by voltages and currents with low total harmonic distortion (THD) levels less than 5%.[5] As the actions to improve the quality of an inverter require additional system parts that cause increasing design density, cost, and complexity, the design of the inverter is quite important considering the optimality criterion.[6]

Various type three-phase inverters based on pulse width modulation (PWM)[7–9] and pulse amplitude modulation (PAM)[10–12] techniques are studied well in the literature for decades. Because of the easy application and control of these PWM- and PAM-type inverters, considerable numbers of studies are done for these inverters. Although the advantage of obtaining the desired output voltages without the dependence on output parameters, the obtained output voltages'

wave forms include considerable THD values, as they are quite far from the ideal sine wave form. Improving techniques to reduce the THD levels such as additional cascade connections and filtering through coupling transformer or passive filters[13] are applied for PWM- and PAM-type inverters. But it is clear that these solutions increase the mentioned design density, cost, and complexity.

Depending on the development of switch-mode power electronics converters in recent decades, switch-mode operation-based inverters are studied and developed by the researchers in the literature. The natural low-pass filtered structure and considerable high switching frequency operation of these switch-mode inverters allow producing low THD level output voltages with considerable close to ideal sine wave forms according to the traditional PWM and PAM type inverters. Although this mentioned advantage, these switch-mode inverters require robust and efficient closed-loop control as the output voltages that are desired at the inverter outputs are quietly dependent on the output loads and other system parameters that may be change in any time of the inverters operations. The switch-mode inverter topologies are developed through the reorganizing of the direct current-direct current (DC-DC) converters to be able to produce alternative voltages. Although buck-,[14–16] boost-,[17–20] buck-boost-,[21–24] and Ćuk-type[25–27] switch-mode single-phase inverters in quite numbers are successfully developed, the limited numbers of three-phase switch mode inverters find place in the literature with such as buck,[28,29] boost,[30,31] and Ćuk[32,33] types. Buck-boost-type switch-mode three-phase inverters are also studied in the literature, and a comparative brief analysis of these studies is given in the below paragraph.

De Brito and Canesin[34] propose a buck-boost-type three-phase grid-connected inverter for photovoltaic (PV) systems. De Brito et al.[35] present the same study with small additions. The inverter output connected to the grid is wye-connected, but neutral return is absent in the topology. So the inverter can operate only on balanced conditions with just same as the grid frequency. The topology includes seven active switches, six diodes, one inductor, and three capacitors. The components of the topology are considered as ideal, so the real parasitic components of them are ignored in the study. The dynamic equations are given, but the detailed dynamic analysis is not done. Any information about the inverter control is not presented. Diab et al.[36] present a wye-connected topology for general purpose of supplying three-phase loads. Because of the absence of the neutral return, the inverter can supply only balanced three-phase loads. The topology is built by six active switches, three inductors, and three capacitors. The inverter components are assumed as ideal without considering the real parasitic components. The dynamic analysis of the inverter is not given. A nonlinear sliding mode control is applied to the inverter system, but the controller design is not given. Jianlin et al.[37] proposed the same topology in Diab et al.[36] with the same considerations and lack of dynamic analysis; just a double-loop-based PI controller is used for the feedback control of the inverter. But same as in Diab et al.,[36] the design information of the control system is absent in Jianlin et al.[37] Antivachis et al.[38] proposed a wye-connected inverter for motor control with a topology consists of 12 active switches, 3 inductors, and 4 capacitors. The components of the topology are considered as ideal, and the inverter dynamic analysis is not given. PI controller is used for the feedback control, but the design of the controller is not presented. The proposed z-source inverter by Cavalcanti et al.[39] is developed for general purpose for supplying of the three-phase loads. The existence of the neutral return enables the inverter operation in unbalanced load conditions. Same as the mentioned similar studies, the real parasitic components of the inverter topology elements are ignored. The dynamic analysis is given in the study, and big-signal transfer function of the inverter is obtained. But small-signal transfer function is not derived. PI controller is applied for the feedback control, and the controller design is given detailed.

In this study, a novel buck-boost-type three-phase inverter for general purpose with a novel hybrid control which is patented by Yalcin[40] is presented. The inverter topology is built in moderate numbers of the elements by only 3 capacitors, 3 inductors, and 24 active switches with neutral return. Although some of the existing similar studies in the literature have less numbers of elements according to the proposed inverter topology, it must be noted that the proposed inverter has superior and advantageous features than the existing inverter topologies as described as follows. The neutral return provides balanced and unbalanced three-phase inverter operations. The buck-boost-based structure of the inverter enables obtaining wide range of output voltages amplitudes lower or higher than the input direct voltages. Unlike the similar studies in the literature, the proposed three-phase inverter has a modular structure that the output phases can be controlled independently in terms of phase voltage amplitudes and phase frequencies for three independent single-phase inverter operations. Snubber cells that provide soft switching of the active switches used in the inverter circuit are built. Additionally, apart from the existing studies in the literature, a novel inverter control method that is open-loop assisted closed-loop hybrid control is developed. The developed hybrid control method improves the performance of the response for tracking the reference ideal sine wave forms in a robust and an efficient manner while

the change of inverter mathematical model during the transitions between various operation parameters. The detailed dynamic analysis considering the real parasitic components of the elements in the topology is done to obtain accurate results in practical operation. The small-signal transfer function and Bode diagram analyses are also obtained for the study to be used in hybrid control design. The simulation tests are applied to the proposed three-phase buck-boost-type inverter in MATLAB-Simulink to prove the theoretical accuracy. In order to prove the real-time practical accuracy of the proposed inverter, an experimental laboratory setup is built for 0–50 Hz, 0–100 Vp, and 1.5 kW operation values. Both the simulation and the experimental results demonstrate that the proposed three-phase buck-boost-type inverter can meet the mentioned operation requirements with high-quality output voltage THD levels under 5% on different working points.

In Table 1, a brief comparison between the proposed inverter study and the similar studies of switch-mode buck-boost three-phase inverter studies in the literature is given regarding the capabilities of unbalanced operation and independent single-phase operation, capability of operation in different output frequencies, converter components number, capability of supplying output load type, including snubber cells, inverter control technique, and taking into account of parasitic effects of the topology components.

As seen from Table 1, the number of the total elements used in the proposed inverter topology is a little higher than the existing inverter topologies. But it must be noted that the proposed inverter has superior capabilities and advantages regarding inverter operation features according to the similar existing ones in the literature. On the other hand, it also must be noted that the passive elements number of the proposed inverter (the inductors and the capacitors) is equal to[36,37] or lower than[38,39] the compared ones where the passive components cause more density and cost according to the active switches. Thus, the proposed inverter topology includes moderate number of elements regarding reduced cost and density with enhanced operation capabilities according to the similar inverter topologies in the literature that have limited operation capabilities as seen from Table 1.

In Section 2, the main topology, snubber cells design, and detailed dynamic analysis of the proposed inverter are given. Section 3 determines the proposed open-loop assisted closed-loop hybrid control method for the inverter operation. In Section 4, the inverter design and the results of both the simulation and the experimental tests on the proposed inverter are presented. Section 5 draws the conclusion of the paper.

2 | THE PROPOSED THREE-PHASE BUCK-BOOST INVERTER

The topology and the operation procedure of the proposed inverter are given detailed in this section. The built snubber cells of the active switches through the main inverter circuit are demonstrated in the section. The detailed dynamic analysis of the topology is also derived. The inverter's small-signal transfer function is obtained through the dynamic analysis for the proposed hybrid control method in future sections.

2.1 | Three-phase buck-boost inverter topology

The main topology of the proposed three-phase buck-boost inverter can be represented in Figure 1.[40] As seen from Figure 1, three independent subcircuit-based buck-boost converters comprise the proposed three-phase buck-boost inverter. The subscripts "1, 2, 3" seen in Figure 1 indicate the three phases, and they are represented generally by the subscript "n" where $n = 1, 2, 3$. U_{o_n} and U_{i_n} represent the output three-phase alternative voltages and the input direct voltages of the inverter, respectively. The input voltages U_{i_n} are supplied from pure direct voltages E_n in the study. But in practice, the input voltages may be supplied by time variant direct voltage sources. U_{S_n} determines the voltages between the S_{5_n} switches and L_n inductors. The inverter system's neutral point is determined by N. The converters' capacitors are represented by C_n. S, which is the switches on the inverter circuit, defines the solid-state active switches. S_{1_n}, S_{2_n}, S_{3_n}, and S_{4_n} define the unidirectional active switches where S_{5_n} and S_{6_n} define the bidirectional active switches. The active switches are considered as IGBTs in this study. Thus, the proposed inverter circuit with IGBTs that have antiparallel diodes in the bodies can be demonstrated in Figure 2. As demonstrated in Figure 2, S_{5_n} and S_{6_n} bidirectional switches are built by two IGBTs connected back to back. Z_n determines the three-phase load impedances with wye connection. The load neutral points of the inverter subcircuits and the three-phase load neutral are connected together to provide a neutral return. Thus, three-phase unbalanced or three independent single-phase modular operations are provided for the proposed inverter.

TABLE 1 The brief comparison between the proposed switch mode buck-boost type three phase inverter and the similar existing inverter studies

Study	Capability of unbalanced operation	Capability of independent single phase operation	Capability of frequency change	Capability of supplying output load	Including Snubber cells	Control technique	Topology model	Switches number		Passive elements number	
								Active switch	Diode	Inductor	Capacitor
Proposed	Yes	Yes	Yes	Ohmic/ inductive/ capacitive	Yes	PID + open-loop control	Real parasitic	24	-	3	3
[34]	No	No	No	Only GC	No	N^G	Ideal	7	6	1	3
[35]	No	No	No	Only GC	No	NG	Ideal	7	6	1	3
[36]	No	No	Yes	Only Ohmic	No	SMC	Ideal	6	-	3	3
[37]	No	No	Yes	Only Ohmic	No	PI	Ideal	6	-	3	3
[38]	No	No	Yes	3-phase motor	No	PI	Ideal	12	-	3	4
[39]	No	No	Yes	Only Ohmic	No	PI	Ideal	9	-	9	9

Abbreviations: GC, grid connection; NG, not given.

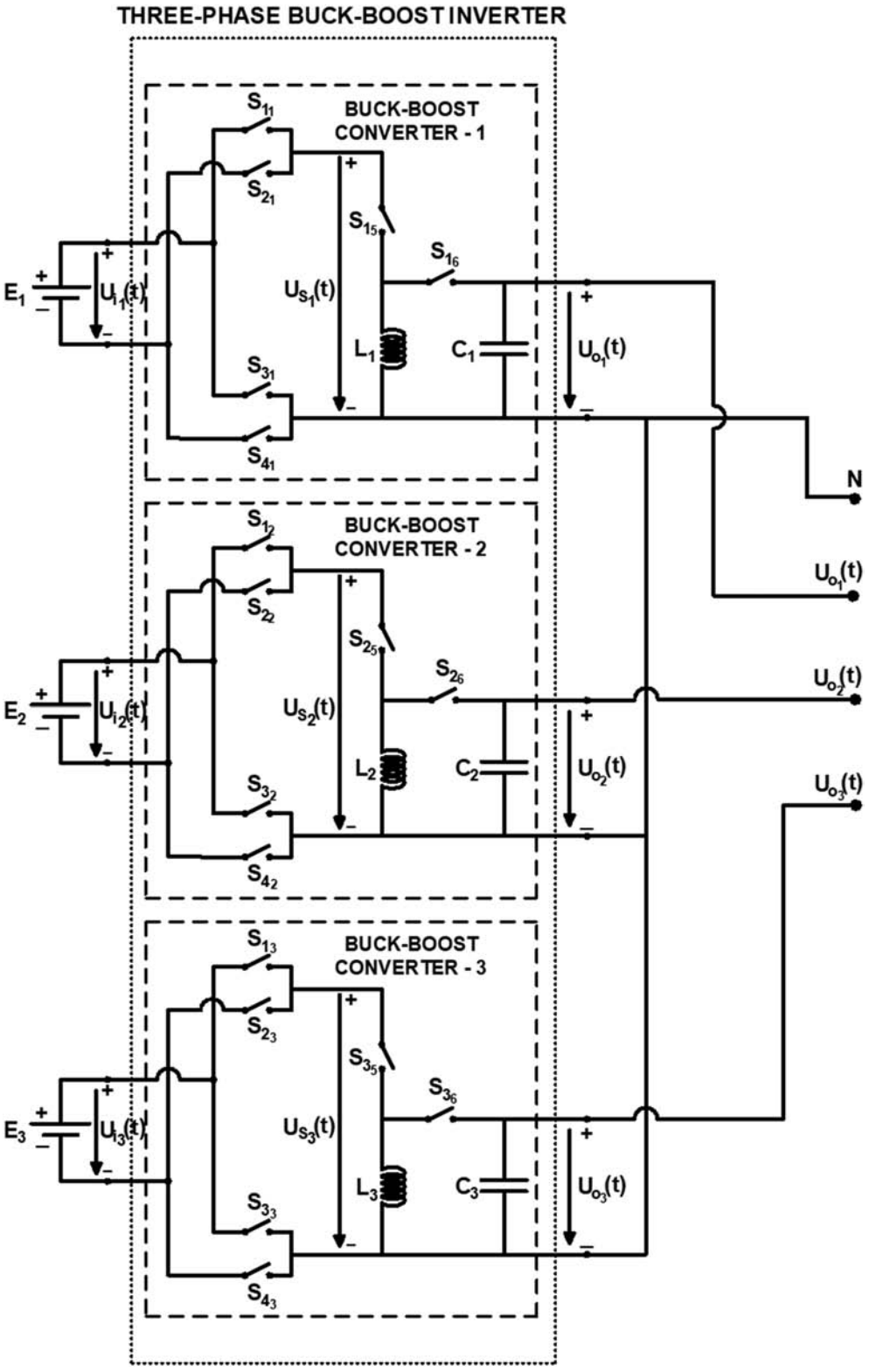

FIGURE 1 General topology of the proposed three-phase buck-boost inverter circuit

2.2 | The proposed inverter's operation fundamentals

The fundamental of the proposed inverter's operation can be determined with the general topology of the inverter circuit shown in Figure 1. Input direct voltages to close to sine-wave output alternative voltages' inversion are obtained

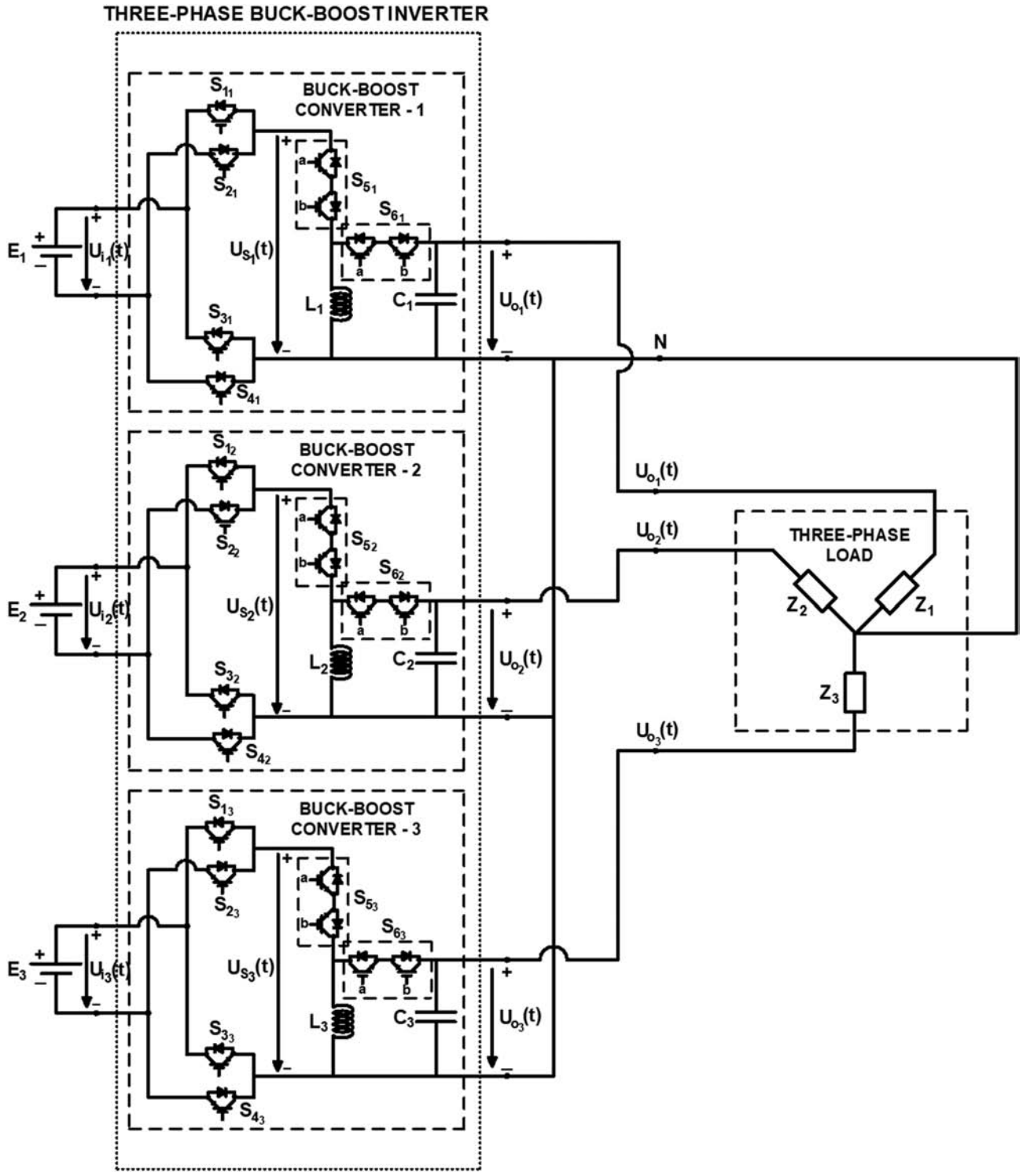

FIGURE 2 The topology of the proposed inverter circuit including IGBTs

through the proper control of the PWM duty ratio of S_{5_n} switches based on the operation procedure of the traditional DC-DC buck-boost converter in terms of the relation between the input and the output.[41] During t_{on} determined by T_S and the PWM duty ratio d, the switches S_{5_n} are turned on, and the switches S_{6_n} are turned off. During the t_{on} period, inverter input voltages V_{i_n} supply and energize the inductors L_n, and the pre-energized capacitors C_n supply the output phase loads Z_n. During t_{off} determined by T_S and the PWM duty ratio d, the switches S_{5_n} are turned off, and the switches S_{6_n} are turned on. During the t_{off} period, the pre-energized L_n supplies both C_n and Z_n. So, by the way of the

proper control of PWM duty ratio d of the switches S_{5_n} continuingly, the phase voltages of the inverter output can be obtained with a close to sine wave form with the magnitudes lower or higher than the input direct voltages magnitudes.

The switches S_{1_n}, S_{2_n}, S_{3_n}, and S_{4_n} are used to determine the polarity of the output phase voltages' half waves for producing alternative voltages. For producing positive half-wave output voltage of any phase output, S_{2_n} and S_{3_n} are turned on when S_{1_n} and S_{4_n} are turned off. For this case, $V_{S_n}(t)$ are obtained identical to $V_{i_n}(t)$ in terms on amplitude but in reverse polarity for the determined polarities. Thus, the phase output voltages $V_{o_n}(t)$ are produced as positive for the determined polarities. For producing negative half-wave output voltage of any phase output, S_{1_n} and S_{4_n} are turned on when S_{2_n} and S_{3_n} are turned off. For this case, $V_{S_n}(t)$ is obtained identical to $V_{i_n}(t)$ in terms on amplitude and the determined polarities. So the phase output voltages $V_{o_n}(t)$ are produced as negative for the determined polarities.

As mentioned before, the bidirectional switches S_{5_n} and S_{6_n} are built with two back-to-back active switches. So the kind of the stages of half-wave output voltage producing that are positive half-wave and negative half-wave that are expressed detailed above determines the control of the bidirectional switches. Table 2 summarizes how to control the S_{5_n} and S_{6_n} bidirectional switches depending on the mentioned output stages.

The IGBTs' switching pattern that controls the operation of the proposed inverter depending on the previously expressed operation procedure on Figure 2 can be shown as in Figure 3. The equivalent subcircuits of the proposed inverter topology given in Figure 2 are demonstrated depending on the control of the active switches for one-cycle sine wave output voltage producing of any phases in Figure 4. Thus, one cycle of output voltage producing operation of the proposed inverter can be explained as a summary by Figures 3 and 4 in two main stages.

Stage 1 ($0 \leq wt < \pi$): the polarity of the desired output voltage of any output phase that is determined by the reference sine-wave voltage is positive in this stage, and this stage is called as positive half-wave stage. S_{2_n} and S_{3_n} are turned on when S_{1_n} and S_{4_n} are turned off in this stage. The control of the IGBTs part of the switches S_{5_n} and S_{6_n} are obtained depending on the proper PWM duty ratio of switch S_{5_n} that is continuously changed and derived by the control system of the inverter. The control procedure of the bidirectional active switches S_{5_n} and S_{6_n} is determined by the switching pattern of the IGBTs that are part of the bidirectional active switches as seen from Figures 3 and 4 and Table 2.

Stage 2 ($\pi \leq wt < 2\pi$): the polarity of the desired output voltage of any output phase that is determined by the reference sine-wave voltage is negative in this stage, and this stage is called as negative half-wave stage. S_{1_n} and S_{4_n} are turned on when S_{2_n} and S_{3_n} are turned off in this stage. Identical to the explanations given in Stage 1, the control of the IGBTs part of the switches S_{5_n} and S_{6_n} are obtained depending on the proper PWM duty ratio of switch S_{5_n} that is continuously changed and derived by the control system of the inverter. The control procedure of the bidirectional active switches S_{5_n} and S_{6_n} are determined by the switching pattern of the IGBTs that are part of the bidirectional active switches as seen from Figures 3 and 4 and Table 2.

2.3 | The snubber cells design of the active switches

The snubber cells are developed for the active switches that are part of the proposed inverter circuit as IGBTs in order to provide soft switching of the mentioned active switches. The developed snubber cells for the IGBTs can be shown in Figure 5 through any phase subcircuit of the proposed inverter demonstrated by Figure 2.

As shown in Figure 5, the snubber cells are developed as parallel polarized resistor-capacitor-diode (RCD) cells and serial polarized resistor-inductor-diode (RLD) cells. These snubber cells provide soft switching of the IGBTs used in the inverter topology during turn-on or turn-off processes. The RLD snubber cells are serial connected to the IGBTs and achieve close to zero current switching when the turn-on processes of the IGBTs are applied. The RCD snubber cells

TABLE 2 Control signal of IGBTs used in Figure 2 as part of bidirectional S_{5_n} and S_{6_n} switches

	S_{5_n}				S_{6_n}			
	Positive half-wave stage		Negative half-wave stage		Positive half-wave stage		Negative half-wave stage	
State	S_{5an}	S_{5bn}	S_{5an}	S_{5bn}	S_{6an}	S_{6bn}	S_{6an}	S_{6bn}
On	Off	On	On	Off	On	Off	Off	On
Off	Off	Off	Off	Off	Off	Off	Off	Off

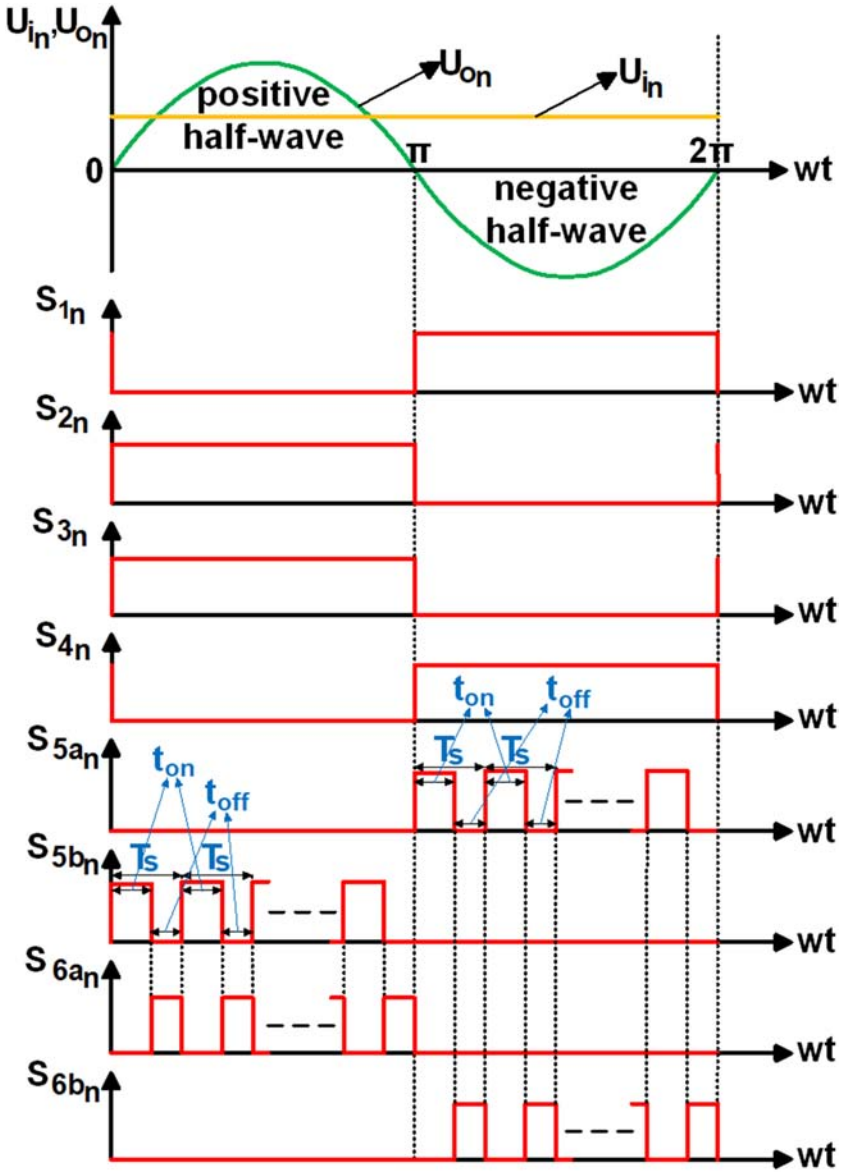

FIGURE 3 The switching pattern of the IGBTs [Colour figure can be viewed at wileyonlinelibrary.com]

are parallel connected to the IGBTs and achieve close to zero voltage switching when the turn-off process of the IGBTs are applied. Thus, soft switching conditions of the switches are obtained for both turn-on and turn-off transitions. The achieved soft switching advantages by the developed snubber cells provide moving away the IGBTs' switching losses from the switches to the snubber cells. However, the RCD snubbers also reduce the voltage pikes on the IGBTs on the turn-off processes that protect the IGBTs from damages of overvoltage. In this way, healthy operation of the inverter is achieved through preventing the dangerous voltage and heating limits of the IGBTs. On the other hand, this must be noted that the snubber cells cannot prevent the IGBTs' switching losses and they can only protect the IGBTs from the damages of the overheating caused by the switching losses through the displacement of the losses from the IGBTs to the snubber cells.

2.4 | The proposed inverter's detailed dynamic analysis

This section derives the proposed inverter's detailed dynamic analysis. The proposed inverter topology with IGBTs seen in Figure 2 is used for the dynamic analysis. As the effect of the snubber cells is nearly zero on the inverter operation,

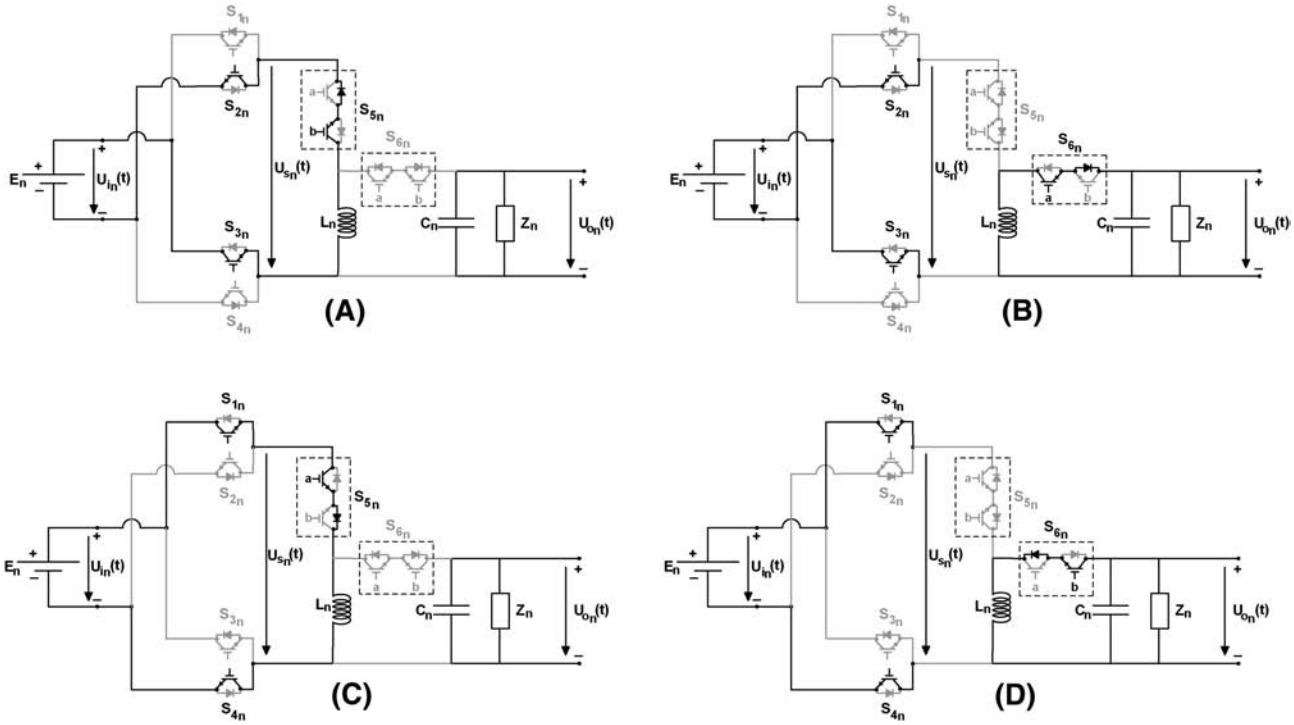

FIGURE 4 The equivalent subcircuits of the proposed buck-boost type inverter: (A) positive half-wave output stage, on-mode (S_{5_n} is on, and S_{6_n} is off); (B) positive half-wave output stage, off-mode (S_{5_n} is off, and S_{6_n} is on); (C) negative half-wave output stage, on-mode (S_{5_n} is on, and S_{6_n} is off); (D) negative half-wave output stage, off-mode (S_{5_n} is off, and S_{6_n} is on)

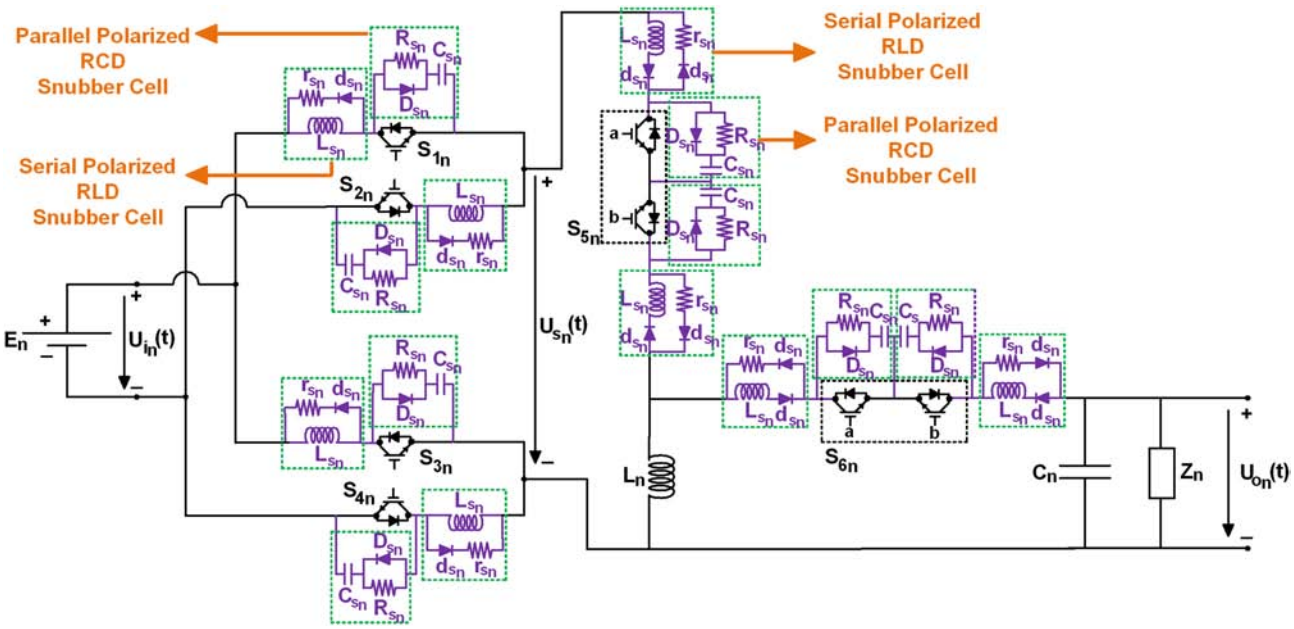

FIGURE 5 The developed snubber cells of the IGBTs in the proposed inverter circuit [Colour figure can be viewed at wileyonlinelibrary.com]

the inverter with snubber cells seen in Figure 5 is not used for the dynamic analysis. The active and passive elements' real parasitic effects are taken into account in Figure 2 to obtain accurate analysis of the dynamic calculations for real-time applications.

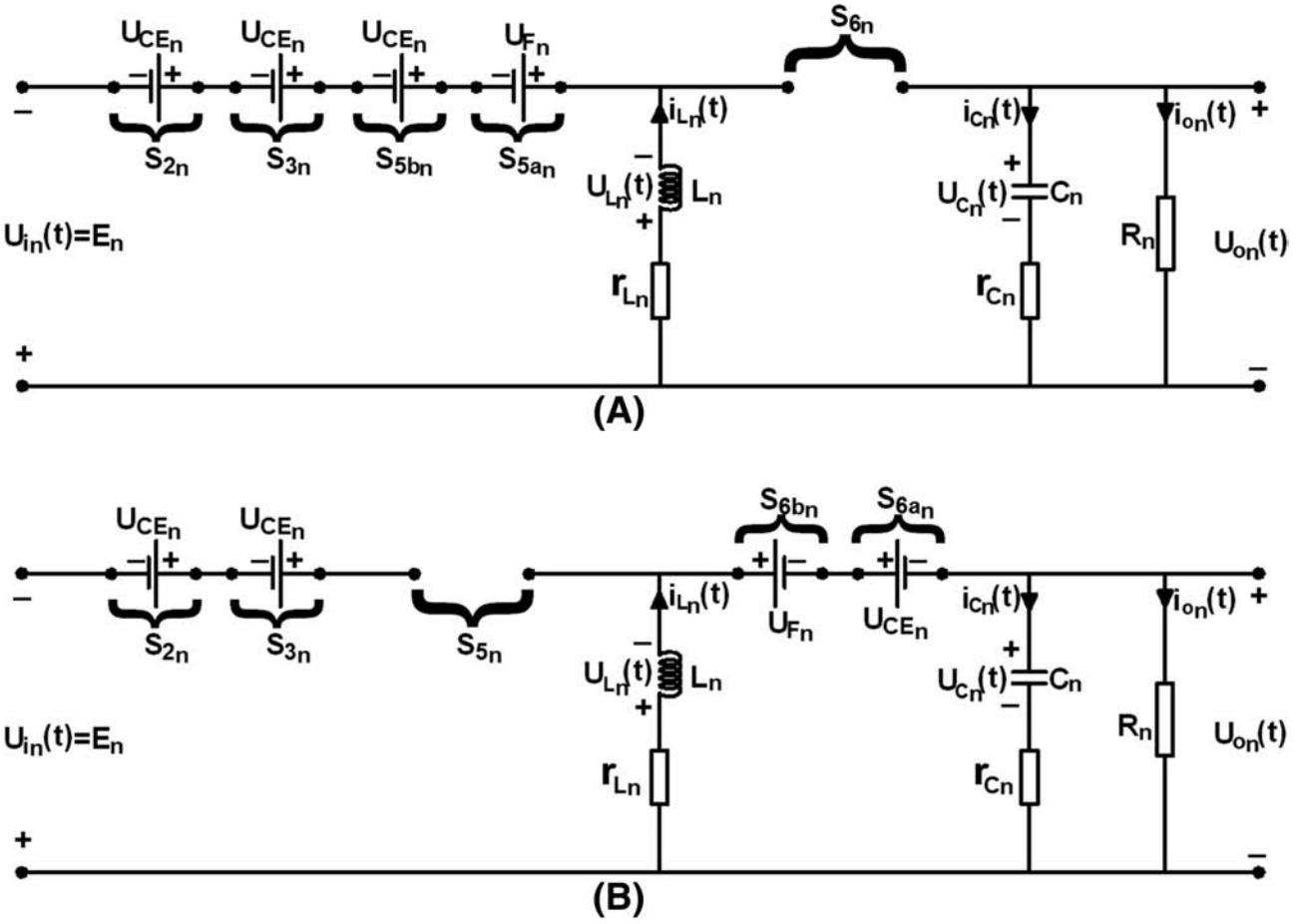

FIGURE 6 The positive half-wave stage equivalent circuit of the inverter (A) on-mode (S_{5_n} is turned on, and S_{6_n} is turned off); (B) off-mode (S_{5_n} is turned off, and S_{6_n} is turned on)

The equivalent circuit of the inverter for one of the subcircuits related to the phase can be shown for positive half-wave stage as in Figure 6. The similar passive and active components used in the subcircuits for each phases are designed as the same. The IGBTs are also chosen as the same for all subcircuits.

In Figure 6, $i_{o_n}(t)$ indicates the output currents of the phases, R_n indicates the output resistive loads of the phases, r_{C_n} indicates the capacitors' equivalent series resistances (ESRs), r_{L_n} indicates the inductors' ESRs, $U_{C_n}(t)$ indicates the voltages of the capacitors, $i_{C_n}(t)$ indicates the currents of the capacitors, $U_{L_n}(t)$ indicates the voltages of the inductors, $i_{L_n}(t)$ indicates the currents of the inductors, U_{CE_n} indicates the voltages of the IGBTs' between collectors and emitters, and U_{F_n} indicates the forward biasing voltages of the IGBTs' reverse parallel body diodes.

The dynamic equations of the proposed inverter for the determined on and off modes shown in Figure 6 can be achieved during the stage of positive half-wave producing from Figure 6. The dynamic analysis achievement of the state variables that are the inductor currents and the output voltages is determined by the two modes indicated in Figure 6 as below.

On-mode (S_{5_n} is turned on, and S_{6_n} is turned off): the Kirchhoff's voltage law (KVL) equation can be achieved through the equivalent circuit's left side seen in Figure 6A as follows.

$$-U_{i_n}(t) + r_{L_n} i_{L_n}(t) + L_n \frac{di_{L_n}(t)}{dt} + 3U_{CE_n} + U_{F_n} = 0. \tag{1}$$

The inductors' current state equation for on-mode can be achieved from 1 as

$$\frac{di_{L_n}(t)}{dt} = -\frac{1}{L_n} r_{L_n} i_{L_n}(t) + \frac{1}{L_n}[U_{i_n}(t) - 3U_{CE_n} - U_{F_n}]. \tag{2}$$

The KVL and Kirchhoff's current law (KCL) equations given below are achieved through the left side and right side of the equivalent circuit seen Figure 6A.

$$i_{C_n}(t) = -i_{o_n}(t), \tag{3}$$

$$C\frac{dU_{C_n}(t)}{dt} = i_{C_n}(t), \tag{4}$$

$$U_{C_n}(t) + i_{C_n}(t) r_{C_n} = U_{o_n}(t), \tag{5}$$

$$i_{o_n}(t) = \frac{U_{o_n}(t)}{R_n}. \tag{6}$$

The output voltages' state equation for on-mode can be achieved through solving 3–6 together as

$$\frac{dU_{o_n}(t)}{dt} = -\frac{1}{R_n C_n\left(1 + \frac{r_{C_n}}{R_n}\right)} U_{o_n}(t). \tag{7}$$

Off-mode (S_{5_n} is turned off, and S_{6_n} is turned on): the KVL equation can be achieved through the equivalent circuit's left side seen in Figure 6b as follows.

$$L_n \frac{di_{L_n}(t)}{dt} + r_{L_n} i_{L_n}(t) + U_{o_n}(t) + U_{CE_n} + U_{F_n} = 0. \tag{8}$$

The inductors currents' state equation for off-mode can be achieved from 8 as

$$\frac{di_{L_n}(t)}{dt} = -\frac{1}{L_n} r_{L_n} i_{L_n}(t) - \frac{1}{L_n} U_{o_n}(t) - \frac{1}{L_n}(U_{CE_n} + U_{F_n}). \tag{9}$$

The KVL and KCL equations given below are achieved through the left side and right side of the equivalent circuit seen Figure 6B.

$$i_{L_n}(t) = i_{C_n}(t) + i_{o_n}(t), \tag{10}$$

$$U_{C_n}(t) + i_{C_n}(t) r_{C_n} = U_{o_n}(t), \tag{11}$$

$$U_{L_n}(t) + r_{L_n} i_{L_n}(t) + U_{o_n}(t) + U_{CE_n} + U_{F_n} = 0, \tag{12}$$

$$i_{o_n}(t) = \frac{U_{o_n}(t)}{R_n}. \tag{13}$$

The output voltages' state equation for off-mode can be achieved through solving 10–13 together as

$$\frac{dU_{o_n}(t)}{dt} = \frac{R_n}{R_n + r_{C_n}}\left[\frac{1}{C_n} - \frac{r_{C_n} r_{L_n}}{L_n}\right] i_{L_n}(t) - \frac{R_n}{R_n + r_{C_n}}\left(\frac{r_{C_n}}{L_n} + \frac{1}{R_n C_n}\right) U_{o_n}(t) - \frac{R_n}{R_n + r_{C_n}} \frac{r_{C_n}}{L_n}(U_{CE_n} + U_{F_n}). \tag{14}$$

The equation of the state-space model for on-mode can be achieved through 2 and 7 as follows:

$$\begin{bmatrix} \dot{i}_{L_n}(t) \\ \dot{U}_{o_n}(t) \end{bmatrix} = \begin{bmatrix} -\frac{1}{L} r_{L_n} & 0 \\ 0 & -\frac{1}{(R_n + r_{C_n}) C_n} \end{bmatrix} \begin{bmatrix} i_{L_n}(t) \\ U_{o_n}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_n} & -\frac{3}{L_n} & -\frac{1}{L_n} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} U_{i_n}(t) \\ U_{CE_n} \\ U_{F_n} \end{bmatrix}. \tag{15}$$

The equation of the state-space model for off-mode can be achieved through 9 and 14 in a similar manner as follows:

$$\begin{bmatrix} \dot{i}_{L_n}(t) \\ \dot{U}_{o_n}(t) \end{bmatrix} = \begin{bmatrix} -\frac{1}{L} r_{L_n} & -\frac{1}{L_n} \\ \frac{R_n}{R_n + r_{C_n}}\left[\frac{1}{C_n} - \frac{r_{C_n} r_{L_n}}{L_n}\right] & -\frac{R_n}{R_n + r_{C_n}}\left[\frac{r_{C_n}}{L_n} + \frac{1}{R_n C_n}\right] \end{bmatrix} \begin{bmatrix} i_{L_n}(t) \\ U_{o_n}(t) \end{bmatrix} + \begin{bmatrix} 0 & -\frac{1}{L_n} & -\frac{1}{L_n} \\ 0 & -\frac{R_n}{R_n + r_{C_n}} \frac{r_{C_n}}{L_n} & -\frac{R_n}{R_n + r_{C_n}} \frac{r_{C_n}}{L_n} \end{bmatrix} \begin{bmatrix} U_{i_n}(t) \\ U_{CE_n} \\ U_{F_n} \end{bmatrix}. \tag{16}$$

The identical state-space equations with 15 and 16 are achieved for negative half-wave stage when the dynamic analysis is done on the derived equivalent circuit for the negative half stage. Thus, the state-space equations achieved by 15 and 16 are valid on all stages of the inverter operation.

The achieved linearized small-signal transfer function related with the PWM duty ratios of the phase subcircuits and the phase output voltages is derived by the help of 15 and 16 that are the determined state-space equations as

$$G_{conv_n}(s) = \frac{\hat{U}_{o_n}(s)}{d_n(s)} = \frac{g_n s + (a_n g_n + c_n f_n)}{s^2 + (a_n + e_n)s + (a_n e_n - b_n c_n)}. \tag{17}$$

The coefficients in 17 can be expressed as follows:

$$a_n = \frac{r_{L_n}}{L_n}, \tag{18}$$

$$b_n = -\frac{\left(1 - \bar{D_n}\right)}{L_n}, \tag{19}$$

$$c_n = \left(1 - \bar{D}_n\right) \frac{R_n}{R_n + r_{C_n}}\left[\frac{1}{C_n} - \frac{r_{C_n} r_{L_n}}{L_n}\right], \tag{20}$$

$$e_n = \frac{\bar{D_n}}{(R_n + r_{L_n}) C_n} + \left(1 - \bar{D_n}\right) \frac{R_n}{R_n + r_{C_n}}\left(\frac{r_{C_n}}{L_n} + \frac{1}{R_n C_n}\right), \tag{21}$$

$$f_n = \frac{\bar{U_{o_n}} + \bar{U_{i_n}} - 2U_{CE_n}}{L_n}, \tag{22}$$

$$g_n = -\frac{R_n}{R_n + r_{C_n}}\left[\frac{1}{C_n} - \frac{r_{C_n} r_{L_n}}{L_n}\right] \bar{i_{L_n}} - \left[\frac{1}{(R_n + r_{C_n})C_n} - \frac{R_n}{(R_n + r_{C_n})}\left(\frac{r_{C_n}}{L_n} + \frac{1}{R_n C_n}\right)\right] \bar{U_{o_n}} + \frac{R_n}{R_n + r_{C_n}} \frac{r_{C_n}}{L_n}(U_{CE_n} + U_{F_n}). \tag{23}$$

In 19–23, $\bar{D_n}$, $\bar{i_{L_n}}$, $\bar{U_{i_n}}$, and $\bar{U_{o_n}}$ indicate the PWM duty ratios of S_{5_n} switches, the inductor currents, inverter input direct voltages, and the amplitudes of the phase output voltages, respectively, for the determined operating point of the inverter operation. $\bar{i_{L_n}}$ and $\bar{U_{o_n}}$ can be formulated as

$$\bar{i_{L_n}} = \frac{\bar{D_n}\bar{U_{i_n}}}{\left(1 - \bar{D_n}\right)^2 R_n}, \tag{24}$$

$$\bar{U_{o_n}} = \frac{\bar{D_n}\bar{U_{i_n}}}{1 - \bar{D_n}}. \tag{25}$$

3 | THE OPEN-LOOP ASSISTED CLOSED-LOOP HYBRID CONTROL METHOD FOR THE INVERTER OPERATION

This section describes the open-loop assisted closed-loop hybrid control method of the proposed buck-boost type three-phase inverter's operation. The general control diagram of the inverter by the proposed hybrid-method can be presented by Figure 7.

As shown in Figure 7, the requested sine wave phase output voltages are defined by the $\sin w_n t$ sine functions having 120° phase angle differences between each other and the U_{r_n} coefficients. U_{r_n} defines the requested magnitudes of the phase output voltages. U_{r_n} can have the values lower or higher than the inverter input voltages U_{i_n} because of the buck-boost structure of the inverter. w_n indicates the requested angular frequencies, so define f_n that is the desired operation frequencies of the phase output voltages. As expressed before, the proposed inverter can also operate for three independent single-phase operation conditions in addition to the three-phase operation condition. In three-phase operation mode of the inverter, w_n has the values identical to each other. But w_n, which also defines the operation phase frequencies, may have no identical values for single-phase independent operations, and the phase angle differences of the sine functions seen in Figure 7 are insignificant on this operation mode of the inverter. In this way, the output reference phase voltages can be defined with U_{r_n} and sine functions as below:

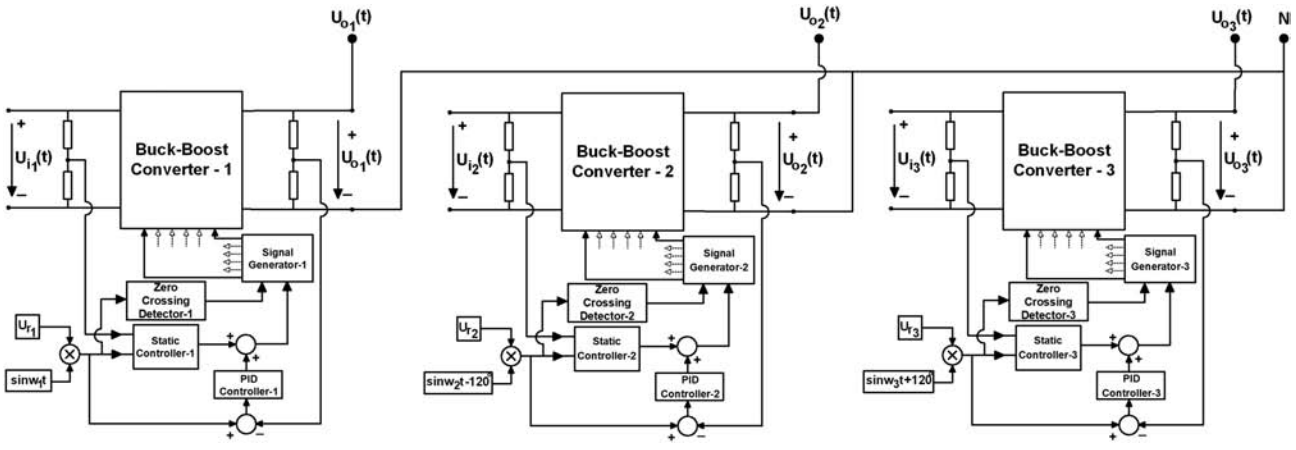

FIGURE 7 The general control diagram of the proposed inverter

$$\left.\begin{aligned} U_{ref_1}(wt) &= U_{r_1}\sin\ w_n t \\ U_{ref_2}(wt) &= U_{r_2}\sin\ (w_n t - 120^o)\ \} \\ U_{ref_3}(wt) &= U_{r_3}\sin\ (w_n t + 120^o) \end{aligned}\right. \tag{26}$$

The signal generators shown in Figure 7 generate the active switches' control signals determined by the inverter operation control. The signal control of S_{1_n}, S_{2_n}, S_{3_n}, and S_{4_n} switches is defined through the zero-crossing detectors to achieve the output phase voltages' alternations regarding the procedure expressed in Section 2.2.

The control of S_{5_n} and S_{6_n} active switches is defined by the PWM duty ratios as explained in Section 2.2. The requested PWM duty ratios that provide obtaining the desired output phase voltages are defined with the help of the proposed hybrid control method. As seen from Figure 7, the proposed hybrid control method is structured with traditional closed-loop control and the open-loop control that assists it. Figure 7 demonstrates that PID-based closed-loop controllers of each control system parts of the phases are assisted with the proposed novel open-loop controllers. As it is expressed in future explanations, the open-loop controllers have static behavior in terms of response. So these open-loop controllers are called as static controllers (SCs) in the study. The closed-loop PID controllers are used to provide the achievement of the desired PWM duty ratios of each subcontrol systems with the purpose of the error elimination between the actual output phase voltages and the reference phase voltages. But, in spite of the error eliminating capability, the PID controllers have slow response performances on fast response requirements because of their dynamic behaviors. In the proposed inverter operation, the output phase voltages are requested to track the output reference phase voltages in sine-wave forms. This means that the values of the reference voltages of the output phase subcircuits always change time to time depending on the sine functions. Besides, the other parameters of the inverter can be forced to change for various operation conditions. So the PID controllers cannot achieve the required fast response performances to provide the output phase voltages of tracking the required output reference phase voltages properly. To overcome this issue, the SCs that are based on open-loop structure are designed to assist the closed loop PID controllers. The SCs that are open-loop controllers generate the feedforward PWM duty ratios of the inverter subcircuits under the consideration of both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) as

$$\left.\begin{aligned} d_{SC_n-CCM}(wt) &= \frac{|\,U_{r_n}\ \sin\ w_n t\,|}{U_{i_n}(wt) + |\,U_{r_n}\ \sin\ w_n t\,|} \\ d_{SC_n-DCM}(wt) &= 1 - \frac{2|U_{r_n}\ \sin\ w_n t|^2\ L_n f_{s_n}}{U_{i_n}(wt)[U_{i_n}(wt) + |U_{r_n}\ \sin\ w_n tv\,|]\,|\,Z_n(wt)\,|} \end{aligned}\right\}. \tag{27}$$

The equations of the PMW duty ratios in 27 that are derived by the SCs for the subinverter systems are structured as algebraic. Thus, the algebraic structure of the SCs provides obtaining the open-loop PWM duty ratios in 27 in a fast manner that augment the response performances of the inverter operation. However, the produced PWM duty ratios by the SC in 27 controllers are determined considering the inverter parameters as ideal. Because of this, the proper inverter operation cannot be obtained by the open-loop SC duty ratios, and the errors between the reference and the real output phase voltages occur. Nonetheless, the proposed SCs produce the open-loop duty ratios nearly to the requested PWM duty ratios with a fast response by the help of the static algebraic structures according to the change rate of the reference sine wave output phase voltages. So the SCs assist the closed-loop PID controllers to achieve the proper inverter operation PWM duty ratios in an improved fast response through the help of the determined open-loop duty ratios by the SCs when the parameters of the inverter are forced to change in any working points. In this way, the inverter operation's proper and requested PWM duty ratios can be achieved through the proposed hybrid control method with the developed SCs and PID controllers as below

$$d_n(wt) = d_{SC_n}(wt) + d_{PID_n}(wt). \tag{28}$$

Discrete time control design is considered of the proposed buck-boost type inverter operation in the study. Thus, the control parts of the inverter system's general control diagram given in Figure 7 are considered in the discrete-time design together with the demonstrated control block diagram shown in Figure 8.

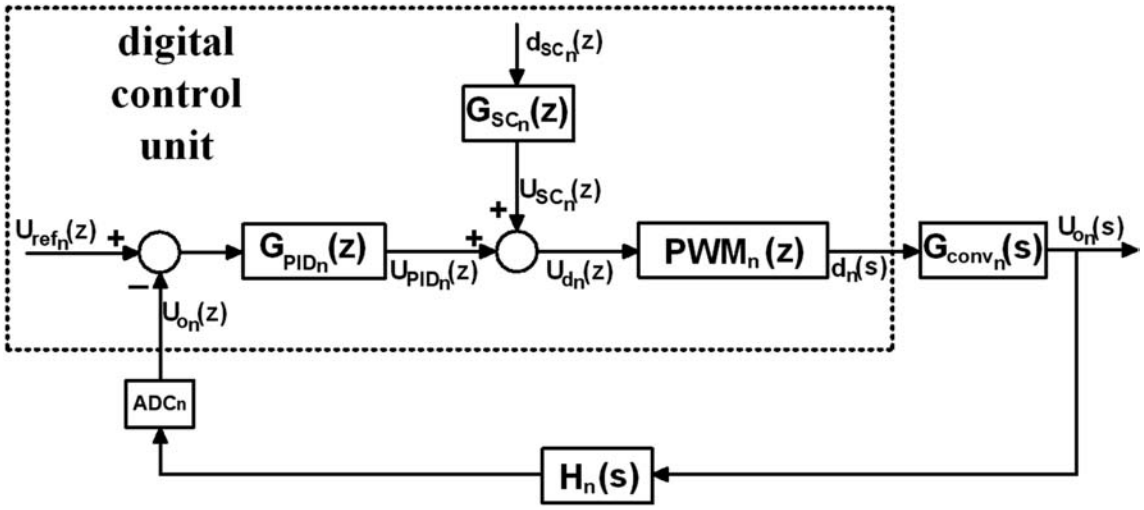

FIGURE 8 The discrete-time control block diagram based on the proposed hybrid control method for the buck-boost-type inverter

As seen from Figure 8, $U_{ref_n}(z)$ indicates the reference output phase voltages' discrete series defined by 26, and they are achieved through the digital control unit. The measurement of the real inverter output phase voltages $U_{o_n}(t)$ is obtained in continuous time through $H_n(s)$ that is the measurement transfer functions, and the measured phase voltages are discretized with the help of the analog-to-digital controllers (ADCs). $d_{SC_n}(z)$ that is the feedforward SCs' duty ratios of each phases in discrete values is directly achieved by the digital control unit through 27. $G_{SC_n}(z)$ indicates the transfer functions related to $U_{SC_n}(z)$ and $d_{SC_n}(z)$. $U_{SC_n}(z)$ indicates the control signals of $d_{SC_n}(z)$ in discrete time that are used to determine the desired phase duty ratios in the PWM stage. $G_{SC_n}(z)$ is defined as follows:

$$G_{SC_n}(z) = \frac{1}{PWM_n(z)}, \tag{29}$$

where $PWM_n(z)$ indicates the PWM processes' transfer functions, which obtain the requested output phases' PWM duty ratios related to $U_{d_n}(z)$ that are PWM processes' total control signals and $d_n(z)$. $G_{PID_n}(z)$ indicates the PID controllers' transfer functions. It can be seen from Figure 8 that $U_{d_n}(z)$ is achieved through the sum of $U_{PID_n}(z)$ that defines the PID controllers' control signals and $U_{SC_n}(z)$ as follows:

$$U_{d_n}(z) = U_{PID_n}(z) + U_{SC_n}(z). \tag{30}$$

The requested PWM duty ratios for each output phases are achieved from Figure 8 as follows:

$$d_n(z) = U_{d_n}(z).PWM_n(z). \tag{31}$$

4 | THE DESIGN OF THE PROPOSED INVERTER AND THE RESULTS OF THE STUDY

The design of the proposed inverter for the inverter operation's test and the results of the study tests are presented in this section. The results of the test studies are achieved by both the simulation and experimental applications in order to prove the theoretical and practical accuracies of the proposals mentioned in previous sections.

4.1 | The design of the proposed inverter

An experimental laboratory setup is purposed to build for 0–50 Hz, 0–100 Vp, and 1.5 kW operation values. Thus, the design criterions and limitations are determined regarding to the purpose. The input direct voltages of each subcircuit phases are chosen in the range of 0–250 V. The output loads for each phase are determined as 2–100 Ω. Hiper-fast IGBTs are chosen for the active switches as IXGH20N60BU1 regarding the defined voltage-power criterions of the inverter with the values of $I_C = 40$ A, $V_{CES} = 600$ V, $V_{CE} = 1.7$ V, and $V_F = 1.6$ V. The identical values of L_n, C_n, and f_{s_n} are selected for each subinverter circuits by the analysis of the inverter's response behavior through 17 as determined in Table 3 with the measured values of ESRs for L_n and C_n.

The parameters of the snubber cells derived by the design for the IGBTs are determined as given in Table 4.

4.2 | The discrete-time PID controller design

The design of the discrete time PID controllers which act as closed-loop unit of the proposed hybrid control method is obtained by the structure demonstrated in Figure 7 and the block diagram of the general control scheme in Figure 8. It is clear that the SCs seem in such a way that they affect like random noises to the control system in Figure 8. Thus, the zero effect assumption of $d_{SC_n}(z)$ is the right way in the design of the discrete-time PID controllers. The parameters of the working point used in the design of the PID controllers are determined as given in Table 5.

Each subinverter circuits' transfer functions can be obtained with the determined parameters by Tables 3–5 as follows:

$$G_{conv_n}(s) = \frac{-1.931 \times 10^6\,\mathrm{s} + 2.008 \times 10^{11}}{\mathrm{s}^2 + 1.425 \times 10^4\,\mathrm{s} + 5.035 \times 10^8}. \tag{32}$$

The values of $H_n(s)$ measurement devices' transfer functions are selected as 0.04. The transfer functions values of the ADCs and the PWM processes are 1. Thus, each subinverter units' open-loop transfer functions excluding the transfer functions of the discrete-time PID controllers can be determined using predetermined transfer functions on Figure 8 as follows:

$$G_n(s) = \frac{-7.723 \times 10^4\,\mathrm{s} + 8.033 \times 10^9}{\mathrm{s}^2 + 1.425 \times 10^4\,\mathrm{s} + 5.035 \times 10^8}. \tag{33}$$

TABLE 3 The chosen values for the switching frequencies, capacitors, and inductors

	Capacitors		Inductors	
Switching frequencies f_{sn} (kHz)	**C_n (μF)**	**r_{Cn} (mΩ)**	**L_n (μH)**	**r_{Ln} (mΩ)**
30	4.7	100	50	150

TABLE 4 The parameters of the IGBTs' snubber cells

RLD Snubber cells			RCD Snubber cells		
L_{Sn} (μH)	**r_{Sn} (mΩ)**	**D_{Sn}**	**C_{Sn} (nF)**	**r_{Sn} (mΩ)**	**D_{Sn}**
1.875	100	1N4007	6.8	150	1 N4007

TABLE 5 The parameters of the working point parameters of the inverter operation

$\bar{U}_{i_n}$ (V)	**$\bar{D}_n$**	**$\bar{U}_{o_n}$ (V)**	**R_n (Ω)**
50	0.667	100	20

The discretized transfer functions of 33 can be obtained regarding the selected switching frequencies as follows:

$$G_n(z) = \frac{1.799\,z + 4.982}{z^2 - 1.197\,z + 0.6219}. \tag{34}$$

The requested general forms of the PID controllers in discrete time can be determined as

$$G_{PID_n}(z) = K_{P_n} + K_{I_n}\frac{z}{z-1} + K_{D_n}\frac{z-1}{z}. \tag{35}$$

The design of the discrete-PID controllers are applied considering the selected optimal overshoot and settling time values by 34 on MATLAB-SISOTOOL interface. The parameters of the PID controllers given by 35 are achieved as below:

$$K_{P_n} = -0.0047,\ K_{I_n} = 0.0137,\ K_{D_n} = 0.0031. \tag{36}$$

Thus, each subinverter units' net open-loop transfer functions can be achieved by 34–36 as follows:

$$T_n(z) = G_n(z).G_{PID_n}(z) = \frac{0.02173\,z^3 + 0.05757\,z^2 - 0.001703\,z + 0.01529}{z^4 - 2.197\,z^3 + 1.819\,z^2 - 0.6219\,z}. \tag{37}$$

The obtained each subinverter circuit control systems' Bode diagrams using 37 are demonstrated in Figure 9. The values of the phase margin (PM) and the gain margin (GM) derived by the Bode-diagram provide well response of the proposed inverter. So the Bode-diagram results prove the design quality of the PID controllers.

4.3 | The applied tests and the results of the simulation studies

In order to demonstrate the theoretical accuracies and efficiencies of the proposed buck-boost inverter through the proposed hybrid control method that are designed before, simulation studies are implemented in MATLAB-Simulink for various test cases determined as in Table 6. The simulation model is built depending on the real-time experimental criterions given detailed in Section 4.1 with the designed controller parameters given in Section 4.2.

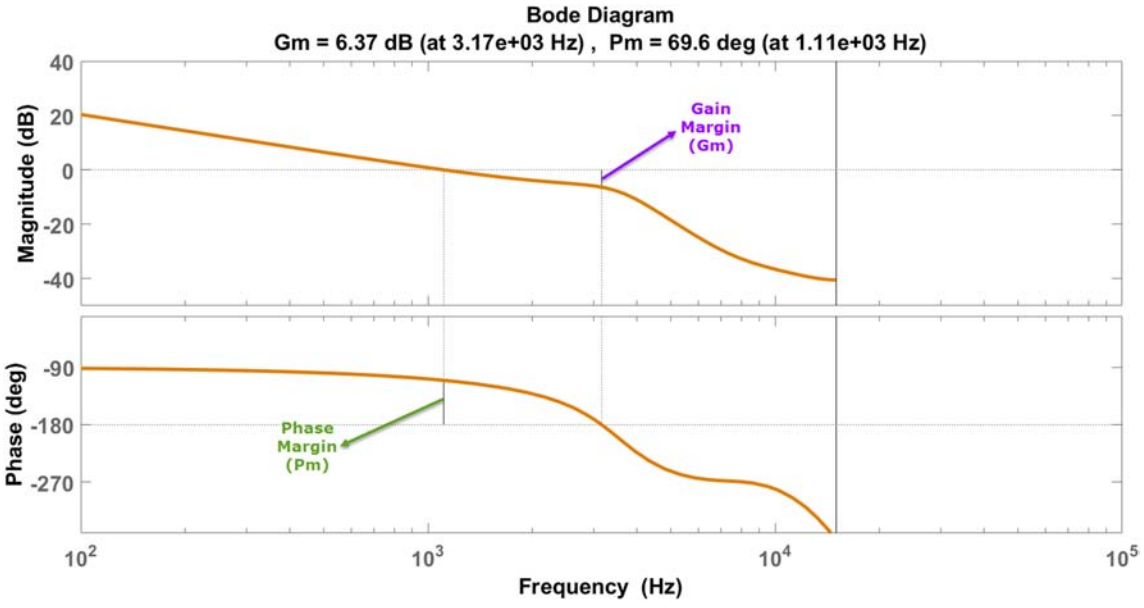

FIGURE 9 The Bode diagram achieved for the control system [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 6 The test cases of the applied studies

Test case no.	U_{in} (V)			Output load Z_n			Desired U_{on} (V)			Desired f_n (Hz)		
	U_{i1}	U_{i2}	U_{i3}	Z_1	Z_2	Z_3	U_{o1}	U_{o2}	U_{o3}	f_1	f_2	f_3
1	140	100	80	Ohm. $R_1 = 20\ \Omega$	Ohm. $R_2 = 20\ \Omega$	Ohm. $R_3 = 20\ \Omega$	100	100	100	50	50	50
2	80	80	80	Ohm. $R_1 = 10\ \Omega$	Ind. $R_2 = 25\ \Omega$ $L_2 = 10$ mH	Cap. $R_3 = 15\ \Omega$ $C_3 = 1$mF	60	100	80	40	40	40
3	75	75	75	Ohm. $R_1 = 30\ \Omega$	Ind. $R_2 = 20\ \Omega$ $L_2 = 5$ mH	Cap. $R_3 = 18\ \Omega$ $C_3 = 0.5$mF	75	90	60	20	30	45

Abbreviations: cap., capacitive load (series connected); ind., inductive load (series connected); ohm., ohmic load.

TABLE 7 The achieved numerical simulation results of the test cases

Test case no	Achieved U_{on} (V)			Achieved f_n (Hz)			THD_{Un} (%)			THD_{In} (%)		
	U_{o1}	U_{o2}	U_{o3}	f_1	f_2	f_3	THD_{U1}	THD_{U2}	THD_{U3}	THD_{I1}	THD_{I2}	THD_{I3}
1	100	100	100	50	50	50	1.064	1.420	1.204	1.064	1.420	1.204
2	60	100	80	40	40	40	1.314	1.609	1.488	1.314	1.470	1.984
3	75	90	60	20	30	45	1.423	1.138	1.329	1.423	1.069	1.569

Three-phase balanced resistive load is requested to be supplied by balanced three-phase voltages in the same frequencies values in Test Case 1. In this case, the input direct voltages of each output phase subcircuits are different. Three-phase unbalanced load with various impedance values and load characteristics is connected to the output of the inverter, and unbalanced three-phase output phase voltages are requested to be obtained in the same operating frequencies at the output in Test Case 2. In this case, the input direct voltages that supply the inverter are considered equal to each other. Independent single-phase loads with various impedance values and load characteristics are connected to each outputs of the three phases in Test Case 3. These single-phase loads are requested to be supplied with desired various phase voltages and phase frequencies when the inverter's input direct voltages are supplied by identical values. The achieved simulation waveforms of the output phase voltages and the output phase currents for the applied test cases on the inverter are demonstrated in Figures 10–12.

The achieved output phase voltages by Figures 10–12 prove the theoretical accuracy and efficiency of the proposed buck-boost type three-phase inverter and the proposed hybrid control method for obtaining nearly to the desired sine-wave output phase voltages on three-phase operation or independent single-phase operation for various working conditions of the inverter. The numerical results of the simulation tests with the voltages and currents' THD values are achieved as shown in Table 7.

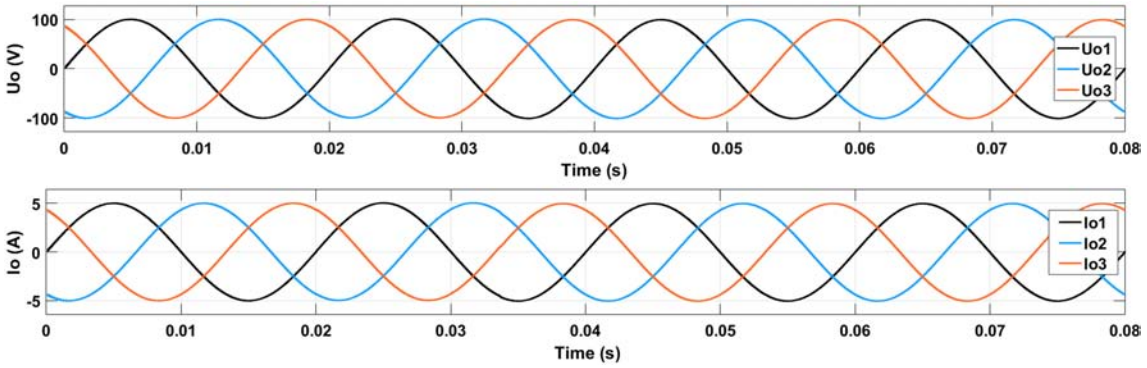

FIGURE 10 The simulation results for Test Case 1 [Colour figure can be viewed at wileyonlinelibrary.com]

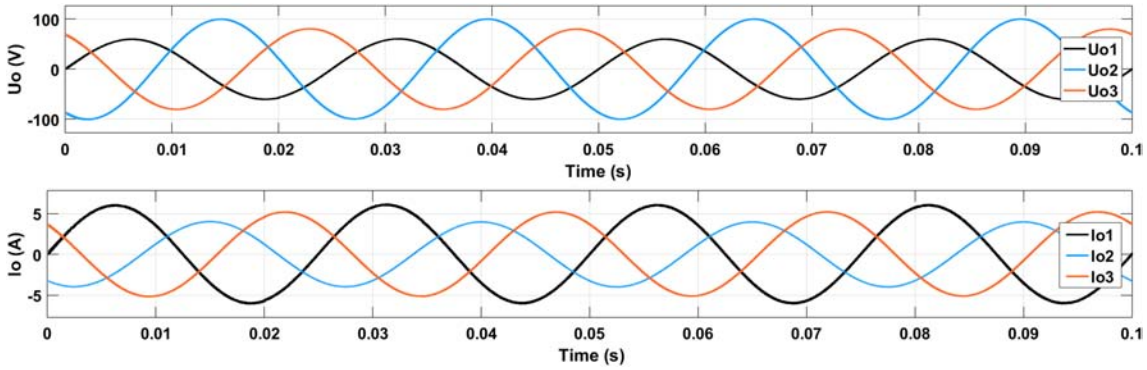

FIGURE 11 The simulation results for Test Case 2 [Colour figure can be viewed at wileyonlinelibrary.com]

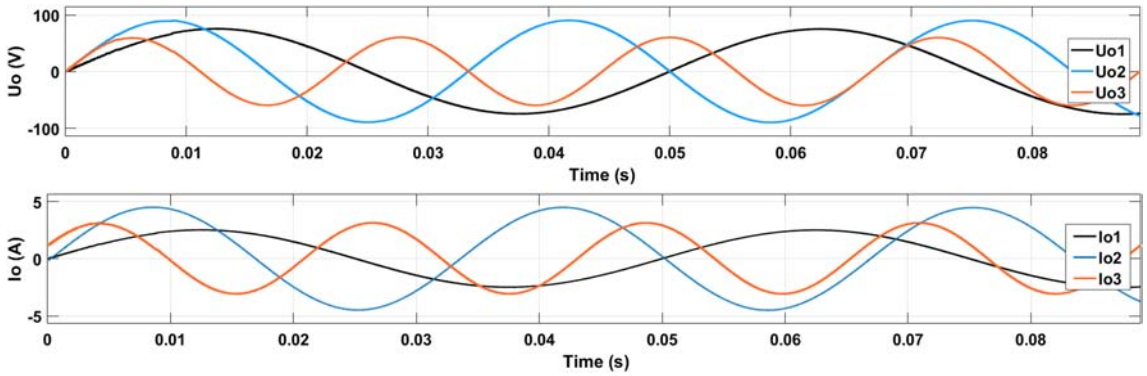

FIGURE 12 The simulation results for Test Case 3 [Colour figure can be viewed at wileyonlinelibrary.com]

As shown in Table 7, the THD values of the output phase voltages (THD_{Un}) are achieved less than 5% in high qualities. Thus, regarding the THD qualities of the output phase voltages, the THD values of the output phase currents (THD_{In}) are also achieved in high qualities. Besides, it draws attention that the THD_{In} values differ from the THD_{Un} ones for the output phases where the capacitive or inductive loads are connected to as the output phase currents are affected by the capacitive and inductive effects of the loads. The capacitive effects increase the harmonics magnitudes of the current harmonics, and the inductive effects decrease the harmonics magnitudes of the current harmonics.

4.4 | The applied tests and the results of the experimental studies

In order to demonstrate the practical accuracies and efficiencies of the proposed buck-boost inverter through the proposed hybrid control method that are designed before, experimental studies are implemented in the built experimental setup for various test cases. The defined test cases for the simulation studies in Figure 5 are used on the experimental test studies to make a comparative analysis between the simulation and the experimental results. The built experimental setup can be demonstrated by Figure 13. The digital control unit in Figure 8 is provided by the PIC32MK1024MCF microcontroller on the experimental setup.

The achieved experimental waveforms of the output phase voltages and the output phase currents for the applied test cases on the inverter are demonstrated in Figures 14–16.

The achieved output phase voltages by Figures 14–16 prove the practical accuracy and efficiency of the proposed buck-boost type three-phase inverter and the proposed hybrid control method for obtaining nearly to the desired sine-wave output phase voltages on three-phase operation or independent single-phase operation for various working conditions of the inverter. The numerical results of the experimental tests with the voltages and currents' THD values are achieved as shown in Table 8. The achievement of the THD results is provided by the oscilloscope wave forms' analyses in the computer through MATLAB.

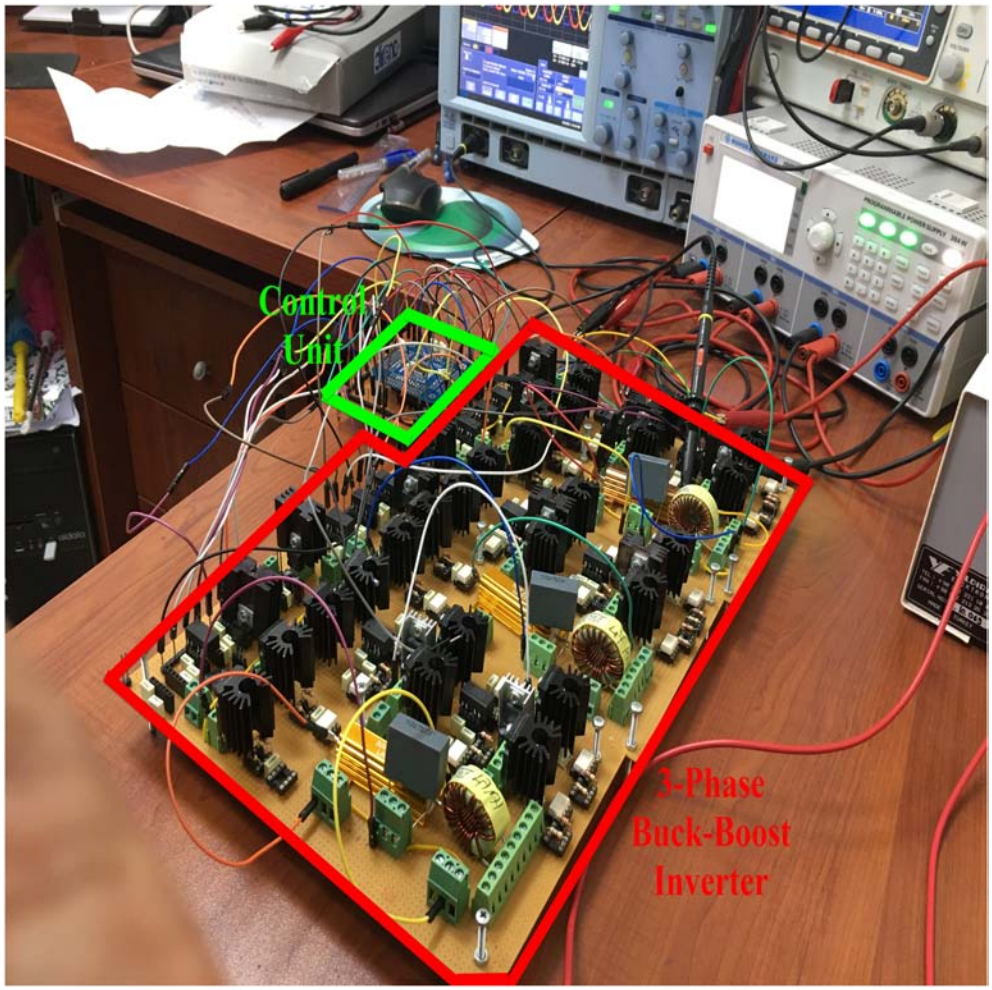

FIGURE 13 The built experimental setup of the inverter system [Colour figure can be viewed at wileyonlinelibrary.com]

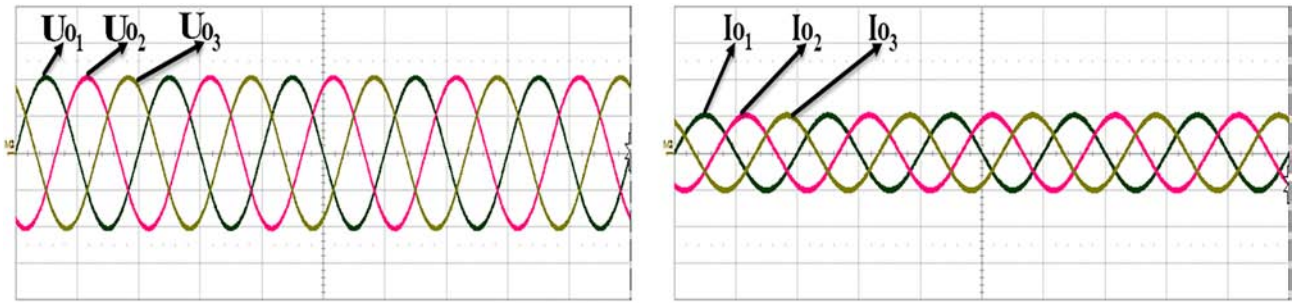

FIGURE 14 The experimental results for Test Case 1 (50 V/div for U_{On}, 5 V/div for I_{On}, and V/div = A/div for Io_n) [Colour figure can be viewed at wileyonlinelibrary.com]

As it can be seen from the numerical results achieved in Table 8, the achieved output phase voltages' and phase working frequencies' values differ from the results obtained in simulation test for the identical test cases. It is clear that the mentioned differences occur because of the unideal components of the practical inverter design. Even so, the values of the related parameters are obtained close to the desired values. In a similar way, the practical inverter circuit's unideal leakage inductances cause the voltages and the currents' THD values in experimental tests to differ from the related THD values achieved in the simulation tests. However, the values of the $THDU_n$ and the $THDI_n$ are achieved in high qualities less than 5% for the practical application.

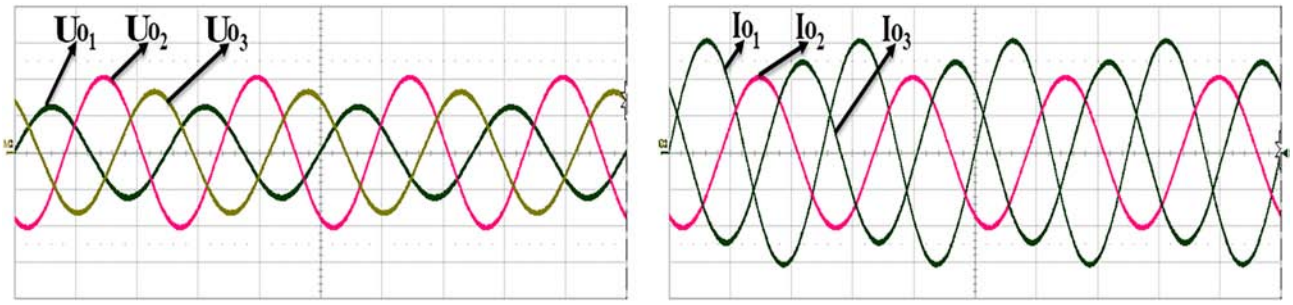

FIGURE 15 The experimental results for Test Case 2 (50 V/div for U_{On}, 2 V/div for I_{On}, and V/div = A/div for Io_n) [Colour figure can be viewed at wileyonlinelibrary.com]

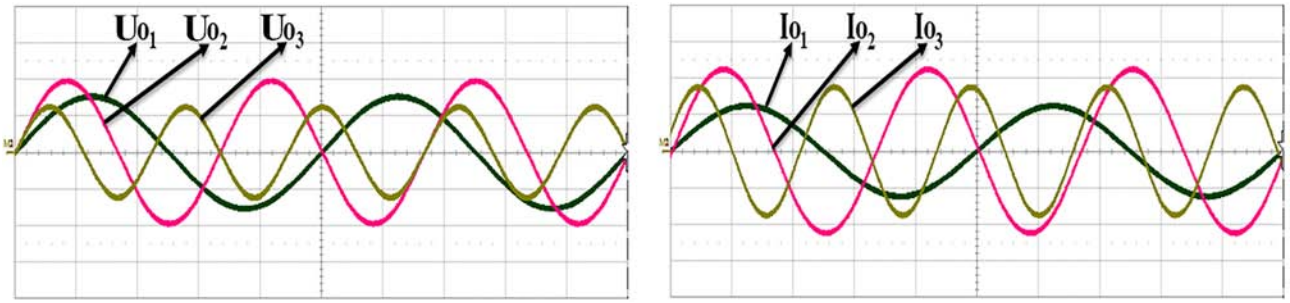

FIGURE 16 The experimental results for Test Case 3 (50 V/div for U_{On}, 2 V/div for I_{On}, and V/div = A/div for Io_n) [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 8 The achieved numerical experimental results of the test cases

	Achieved U_{on} (V)			Achieved f_n (Hz)			THD_{Un} (%)			THD_{In} (%)		
Test case no.	U_{o1}	U_{o2}	U_{o3}	f_1	f_2	f_3	THD_{U1}	THD_{U2}	THD_{U3}	THD_{I1}	THD_{I2}	THD_{I3}
1	99.99	99.96	99.98	49.995	49.989	49.999	1.248	1.665	1.412	1.216	1.624	1.314
2	60.01	99.97	80.02	39.997	39.998	39.994	1.541	1.886	1.745	1.430	1.724	2.006
3	74.96	89.98	60.02	19.997	29.988	24.993	1.654	1.334	1.558	1.538	1.194	1.840

Study	Output voltage THD_I (%)
Proposed inverter	1.194
De Brito et al.[35]	2.9

TABLE 9 The comparison of the output phase currents THD_I results for the proposed inverter and the similar study

A comparison is done between the proposed buck-boost type three-phase inverter and the similar studies in the literature analyzed in the introduction section regarding the THD values in Table 9. The comparison can be done with only one of the similar studies as seen in Table 9, as the mentioned other similar studies do not give any THD results. The comparison of the THD results is provided just only for THDI in Table 9 because of the absence of the THDU results in the compared study. Hence, the comparative results prove the proposed inverter's superiority on obtaining higher-quality THDI than the compared study in the literature.

The $S5_{2a}$ and $S6_{2b}$ switches' switching wave forms on the operation for Test Case 3 including the snubber cells and excluding the snubber cells are demonstrated by Figures 17–20 to reveal the designed snubber cells' soft switching capabilities during the turn-on and the turn-off processes of the used IGBTs in the proposed inverter circuit as an exemplary.

Figures 17 and 18 demonstrate that the RLD snubber cells designed for the IGBTs have the capability of the soft switching achievement during turn-on process that provide nearly zero current switching for the IGBTs which remove

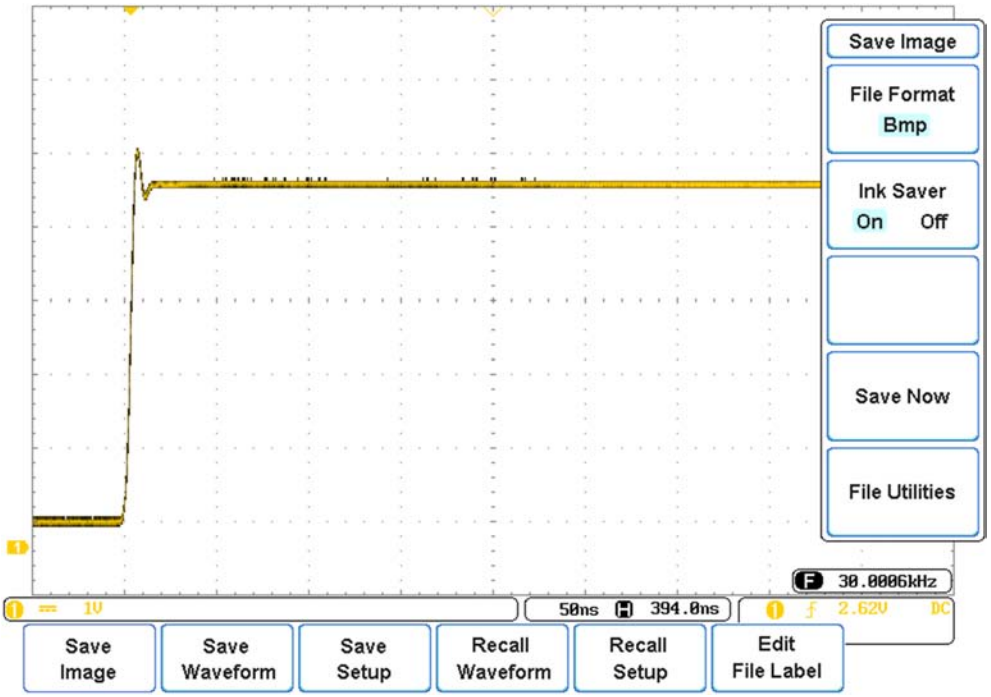

FIGURE 17 The $S6_{2b}$ IGBT's collector-emitter current I_C wave form on Case 3 operation during turn-on process (RLD snubber cell does not exist) (V/div = A/div for I_C) [Colour figure can be viewed at wileyonlinelibrary.com]

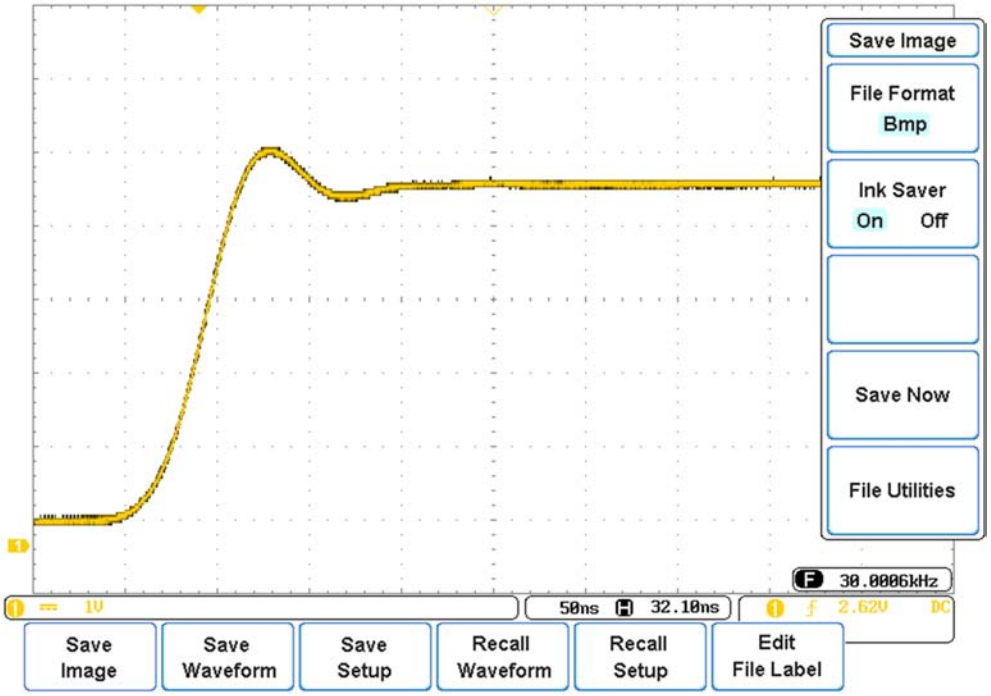

FIGURE 18 The $S6_{2b}$ IGBT's collector-emitter current I_C wave form on Case 3 operation during turn-on process (RLD snubber cell exists) (V/div = A/div for I_C) [Colour figure can be viewed at wileyonlinelibrary.com]

the switching losses from the IGBTs, and thus, they prevent the IGBTs' overheating problems. Likewise, as seen from Figures 19 and 20, the RCD snubber cells designed for the IGBTs have the capability of the soft switching achievement during turn-off process that provides nearly zero voltage switching for the IGBTs which remove the switching losses from the IGBTs. In addition, the RCD snubber cells prevent the overvoltage damages problems through decreasing the IGBTs' overshoot voltages as clearly seen from Figures 19 and 20.

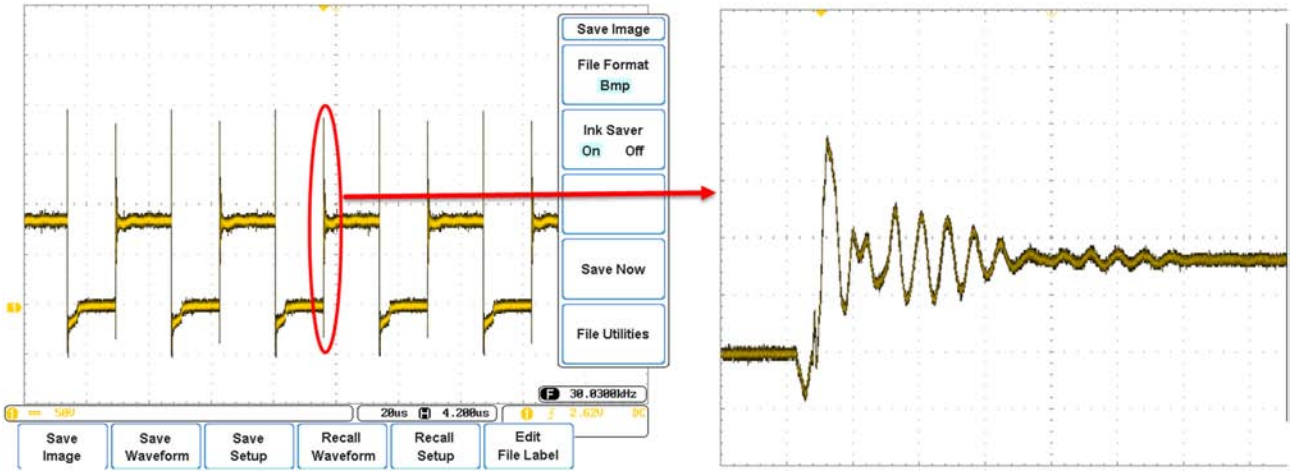

FIGURE 19 The $S5_{2a}$ IGBT's collector-emitter voltage V_{CE} wave form on Case 3 operation during turn-off process (RCD snubber cell does not exist) [Colour figure can be viewed at wileyonlinelibrary.com]

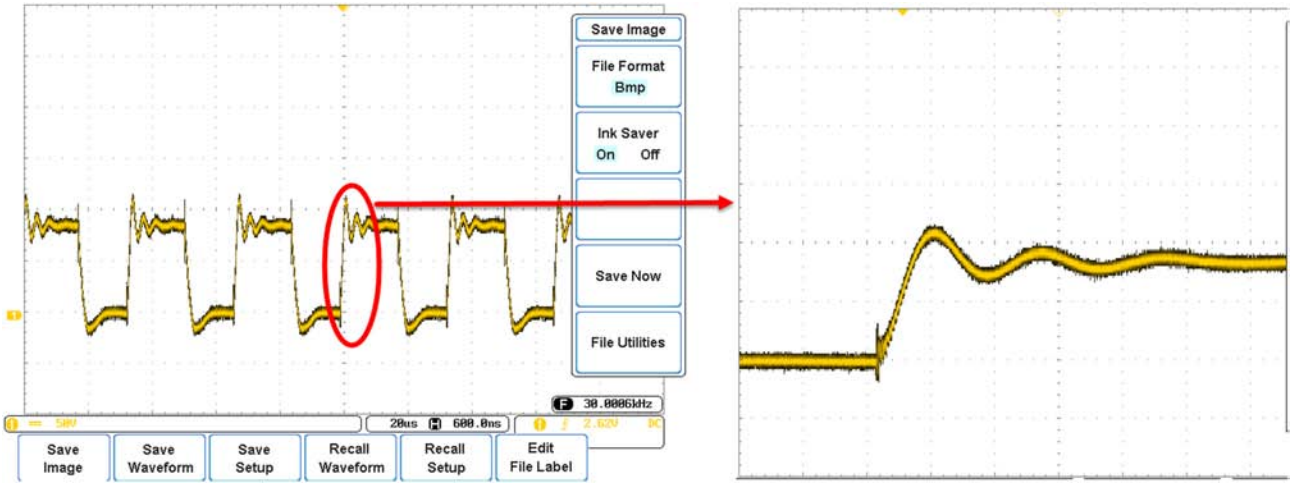

FIGURE 20 The $S5_{2a}$ IGBT's collector-emitter voltage V_{CE} wave form on Case 3 operation during turn-off process (RCD snubber cell exists) [Colour figure can be viewed at wileyonlinelibrary.com]

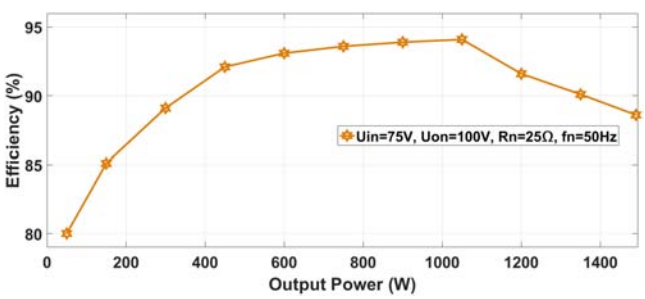

FIGURE 21 The achieved inverter's efficiency curve for different output power rates [Colour figure can be viewed at wileyonlinelibrary.com]

The proposed buck-boost-type inverter's efficiency is obtained for different rates of output power with the upper limit of the maximum power defined in the design process. The inverter's efficiency curve is achieved as presented in Figure 21. As it is seen from Figure 21, until the increase to the half output loading, the efficiency of the inverter system increases. During this stage, it is clear that the individual power loss on the active switches depending on the increase of output loading. But Figure 21 demonstrates that the increase of the power transfer from input the output is more than the increase of the total active switches loss until the output loading is reached to nearly the half rate. As it is again seen from Figure 21, the efficiency of the inverter starts to decrease slightly after the half output loading to the full output loading point, because the increase rate of the active switches' loss starts to lead the total power transfer rate from input to the output. As it is well known the traditional buck-boost converter analysis, the efficiency response seen in Figure 21 is the typical efficiency behavior of the buck-boost converter operation. Nevertheless, the proposed inverter has an average 92% efficiency good enough above the half output loading power rates as seen from Figure 21. As it is explained in Section 2.3, the developed snubber cells for the active switches distribute the switching losses from the switches to the snubbber cells through providing soft switching. Thus, the overheating problem of the switches is prevented, and safety inverter operation is achieved. On the other hand, by this way, the efficiency is enhanced indirectly through decreasing the conduction power losses. Because the conduction resistances of the active switches increase depending on the body heating, so preventing the body heating of the active switches by the snubber cells also helps reducing the conduction power losses that provides increasing efficiency.

A comparison study is applied to prove the efficiency of the proposed open-loop controller supported PID controller-based hybrid control method for various inverter operation points. For this purpose, PID controller without the proposed open-loop controller is applied as standalone for the same test cases given in Table 6 on the applied experimental tests. The experimentally achieved waveforms of Phase 1 voltage Uo1 are shown together on the cases of applying the standalone PID control and the proposed hybrid control method for Test Case 1 separately in Figure 22. It is clear that Test Case 1 parameters are different from the operating point parameters shown in Table 5, which are used for obtaining the PID parameters. Figure 22 proves that the proposed open-loop control supported hybrid controller can track the reference sine wave form more closely than the traditional standalone PID controller. It is clear that the reason of this is the fact that the response performance of the traditional standalone PID controller cannot meet the desired performance as the mathematical model drifts away from the operating point where the PID controller is designed. Thus, the results shown in Figure 22 demonstrates the enhancing effect of the proposed hybrid control technique on the response performance. The similar results are verified for all phase voltages from the oscilloscope analyses for all test cases. The numerical comparative THD_{Un} results of all phase voltages on the applied test cases for the proposed hybrid control method and the traditional standalone PID control technique are given together in Table 10. The results given in Table 10 verify the efficiency of the proposed hybrid control method in terms of the response performance according to the traditional standalone PID technique method for various inverter operation points.

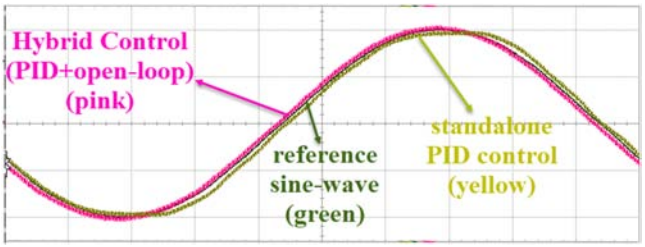

FIGURE 22 Comparative output Phase 1 voltage U_{O1} wave forms of the proposed PID + open-loop hybrid control and the standalone PID control (50 V/div, 2 ms/div) [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 10 Comparative THD_{Un} results for the proposed PID + open-loop hybrid control and the standalone traditional PID control on the test cases

	THD_{Un} (%) results of the proposed PID + feedforward control			THD_{Un} (%) results of the standalone PID control		
Test case no.	THD_{U1}	THD_{U2}	THD_{U3}	THD_{U1}	THD_{U2}	THD_{U3}
1	1.248	1.665	1.412	1.261	1.683	1.427
2	1.541	1.886	1.745	1.557	1.906	1.764
3	1.654	1.334	1.558	1.672	1.348	1.575

5 | CONCLUSION

In this paper, a novel general purpose three-phase buck-boost inverter that consists of moderate number of circuit elements. A novel open-loop assisted closed loop control method is also designed for the proposed study for the aim of improving the inverter operation's response performance for different operation points of the inverter in terms of input direct voltages, requested output phase voltages/frequencies and output phase loads. The buck-boost-based structure of the proposed three-phase inverter provides an opportunity for obtaining wide range of output phase voltages values higher or lower than the inverter's input direct voltage values. Additionally, the proposed inverter topology is designed in a modular structure that provides the opportunity of the inverter operation modes in independent single-phase working and balanced or unbalanced wye-connected three-phase workings. Both simulation and experimental test studies are applied on the proposed inverter to prove the accuracy and the efficiency of the proposals presented in the paper. An experimental laboratory setup is built in 0–50 Hz, 0–100 Vp, and 1.5 kW operation values for the real-time inverter circuit. Simulation tests are also applied for the inverter. The simulation and experimental results achieved by the applied test studies demonstrate the theoretical and the practical accuracy and efficiency of the proposed inverter in producing nearly to sine wave output phase voltages with less than 5% THD rates on the requested frequency operations for various working parameters. The proposed study may lead the researcher to apply the proposed inverter system to specific industrial and power applications. At present, the author has already been studying for developing the proposed inverter system to establish in PV solar systems.

REFERENCES

1. Zhao R, Wang C, Loh PC, Yan Q, Xu H, Blaabjerg F. A practical core loss estimation method for three-phase three-level grid-connected inverters. *IEEE Trans Power Electron*. Mar. 2020;35(3):2263-2267. https://doi.org/10.1109/TPEL.2019.2943875
2. Barzegar-Kalashani M, Tousi B, Mahmud MA, Farhadi-Kangarlu M. Non-linear integral higher-order sliding mode controller design for islanded operations of T-type three-phase inverter-interfaced distributed energy resources. *IET Gener Transm Distrib*. Jan. 2020;14(1):53-61. https://doi.org/10.1049/iet-gtd.2019.0795
3. Kim J, Choi HH, Jung JW. MRAC-based voltage controller for three-phase CVCF inverters to attenuate parameter uncertainties under critical load conditions. *IEEE Trans Power Electron*. Jan. 2020;35(1):1002-1013. https://doi.org/10.1109/TPEL.2019.2912393
4. Rashid MH. *Power Electronics: Circuits, Devices & Applications*. England, UK: Pearson Education Ltd.; 2014.
5. Energylogix, Harmonics and IEEE 519, Denbighshire, Wales. [Online]. Available: http://energylogix.ca/harmonics_and_ieee.pdf, accessed. Accessed: Jan. 10, 2020.
6. Yalcin F, Arifoglu U, Yazici I, Erin K. Robust single-phase inverter based on the buck-boost converter through an efficient hybrid control. *IET Power Electron*. Jan. 2020;13(1):50-59. https://doi.org/10.1049/iet-pel.2019.0913
7. Matsumori H, Shimizu T, Takano K, Ishii H. Three-phase AC filter inductor design for three-phase PWM inverter for conversion efficiency improvement at low load. *Electr Eng Jpn*. Apr. 2018;203(1):37-49. https://doi.org/10.1002/eej.23053
8. Kundu S, Burman AD, Giri SK, Mukherjee S, Banerjee S. Comparative study between different optimisation techniques for finding precise switching angle for SHE-PWM of three-phase seven-level cascaded H-bridge inverter. *IET Power Electron*. Mar. 2018;11(3):600-609. https://doi.org/10.1049/iet-pel.2017.0530
9. Hasanzad F, Rastegar H, Pichan M. A three-dimensional active zero state PWM for common-mode voltage reduction of a three-phase four-leg voltage-source inverter. *World J Eng*. Oct. 2018;15(5):592-603. https://doi.org/10.1108/WJE-12-2017-0423
10. Mohammadi M, Mirzaee A, Magnone P, Moghani J, Mattavelli P. Performance improvement of pulse width-amplitude modulation-based quasi-Z-source inverters: analysis and implementation. *Int J Circuit Theory Appl*. Oct. 2020;48(10):1786-1799. https://doi.org/10.1002/cta.2808
11. Liang WH, Liu YS, Ge BM, Abu-Rub H. Investigation on pulse-width amplitude modulation-based single-phase quasi-Z-source photovoltaic inverter. *IET Power Electron*. Nov. 2017;10(14):1810-1818. https://doi.org/10.1049/iet-pel.2016.0593
12. Yi LZ, Gui QZ, Wang Z. A novel phase-shifted pulse width amplitude modulation for extended-boost quasi-Z source cascaded multilevel inverter based on photovoltaic power system. *J Renew Sustain Energy*. Jan. 2019;11(1):015304. https://doi.org/10.1063/1.5058754
13. Serra FM, Fernández LM, Montoya OD, Gil-González W, Hernández JC. Nonlinear voltage control for three-phase DC-AC converters in hybrid systems: an application of the PI-PBC method. *Electronics*. May 2020;9(5):847. https://doi.org/10.3390/electronics9050847
14. Khan AA, Cha H, Lai JS. Cascaded dual-buck inverter with reduced number of inductors. *IEEE Trans Power Electron*. Apr. 2018;33(4):2847-2856. https://doi.org/10.1109/TPEL.2017.2701400
15. Yang F, Ge H, Yang J, Dang R, Wu H. A family of dual-buck inverters with an extended low-voltage DC-input port for efficiency improvement based on dual-input pulsating voltage-source cells. *IEEE Trans Power Electron*. Apr. 2018;33(4):3115-3128. https://doi.org/10.1109/TPEL.2017.2706762
16. Dai Y, Li W, Zhou C, Zhuang S. Research on transformerless dual-buck full-bridge grid-connected inverter with H5-type for PV systems. *IET Power Electron*. Jan. 2019;12(1):44-50. https://doi.org/10.1049/iet-pel.2018.5196
17. Zhang H, Li W, Ding H, Yi C, Wan X. Observer-pattern modeling and nonlinear modal analysis of two-stage boost inverter. *IEEE Trans Power Electron*. Aug. 2018;33(8):6822-6836. https://doi.org/10.1109/TPEL.2017.2756090

18. Garcia-Rodriguez VH, Silva-Ortigoza R, Hernandez-Marquez E, Garcia-Sanchez JR, Taud H. DC/DC boost converter-inverter as driver for a DC motor: modeling and experimental verification. *Energies*. Aug. 2018;11(8):2044. https://doi.org/10.3390/en11082044
19. Nguyen MK, Tran T. A single-phase single-stage switched-boost inverter with four switches. *IEEE Trans Power Electron*. Aug. 2018;33 (8):6769-6781. https://doi.org/10.1109/TPEL.2017.2754547
20. Flores-Bahamonde F, Valderrama-Blavi H, Bosque-Moncusi JM, Garcia G, Martinez-Salamero L. Using the sliding-mode control approach for analysis and design of the boost inverter. *IET Power Electron*. June 2016;9(8):1625-1634. https://doi.org/10.1049/iet-pel.2015.0608
21. Tang Y, Xu F, Bai Y, He Y. Comparative analysis of two modulation strategies for an active buck-boost inverter. *IEEE Trans Power Electron*. Nov. 2016;31(11):7963-7971. https://doi.org/10.1109/TPEL.2015.2483906
22. Sreekanth T, Lakshminarasamma N, Mishra MK. A single-stage grid-connected high gain buck-boost inverter with maximum power point tracking. *IEEE Trans Energy Convers*. Mar. 2017;32(1):330-339. https://doi.org/10.1109/TEC.2016.2633365
23. Ho CNM, Siu KKM. Manitoba inverter—single-phase single-stage buck-boost VSI topology. *IEEE Trans Power Electron*. Apr. 2019;34(4): 3445-3456. https://doi.org/10.1109/TPEL.2018.2855560
24. Krishnapriya CV, Kochuvila S, and Lekshmi S, Bidirectional buck-boost cascade inverter, in Int. *Conf. Technol. Advanc. Power Eng*, 2015;114-120.
25. Han BC, Kim M, Lee S, and Lee JS, Dynamic modeling and integral sliding mode controller design for the Cuk inverter, in 17th Eur. Conf. Power Electron. Appl., 2015.
26. Mehrnami S, Mazumder SK. Discontinuous modulation scheme for a differential-mode Cuk inverter. *IEEE Trans Power Electron*. Mar. 2015;30(3):1242-1254. https://doi.org/10.1109/TPEL.2014.2314688
27. Wang B, Tang W. A new Cuk-based Z-source inverter. *Electronics*. Nov. 2018;7(11):313. https://doi.org/10.3390/electronics7110313
28. Sun P, Liu C, Lai JS, Chen CL, Kees N. Three-phase dual-buck inverter with unified pulsewidth modulation. *IEEE Trans Power Electron*. Mar. 2012;27(3):1159-1167. https://doi.org/10.1109/TPEL.2011.2164269
29. Sun P, Chen CL, Lai JS, and Liu C, Unified pulse width modulated three-phase four-leg inverter based on dual-buck power cell, in IEEE Energy Convers. Congr. Expo., 2012.
30. Nandi P and Adda R, Generation of switching pulses for three-phase switched boost inverter using space vector modulation, in IEEE Int. Conf. Power Electron. Driv. Energy Syst, 2018.
31. Pati AK, Sahoo NC. A novel power quality enhancement scheme for three-phase differential boost inverter-based grid-connected photovoltaic system with repetitive and feedback linearizing control. *Int Trans Electr Energy Syst*. May 2019;29(5):e2832. https://doi.org/10.1002/2050-7038.2832
32. Rakshit S and Maity J, Three phase, 10 kVA dual conversion type automatic AC voltage regulator—an approach based on fuzzy logic controlled Ćuk converter and PI controlled three phase inverter, in IEEE 8th Power India Int. Conf., 2018.
33. Mehrnami S, Mazumder SK, Soni H. Modulation scheme for three-phase differential-mode Cuk inverter. *IEEE Trans Power Electron*. Mar. 2016;31(3):2654-2668. https://doi.org/10.1109/TPEL.2015.2442157
34. De Brito MAG and Canesin CA, Three-phase tri-state buck-boost integrated inverter, in Int. Conf. Clean Electr. Power, 2013.
35. De Brito M, Sampaio L, Melo G, Canesin CA. Three-phase tri-state buck-boost integrated inverter for solar applications. *IET Renew Power Gener*. Aug. 2015;9(6):557-565. https://doi.org/10.1049/iet-rpg.2014.0072
36. Diab MS, Elserougi A, Abdel-Khalik AS, ElArabawy IF, Massoud AM, and Ahmed S, Non-linear sliding-mode control of three-phase buck-boost inverter, in IEEE 23rd Int. Symp. Ind. Electron, 2014.
37. Jianlin Z, Lidan X, and Shasha L, Double-loop control and stability analysis based on three-phase Buck-Boost inverter, in Int Conf Electr Mach Syst, 2008.
38. Antivachis M, Bortis D, Schrittwieser L, and Kolar JW, Three-phase buck-boost Y-inverter with wide DC input voltage range, in IEEE Appl. Power Electron. Conf. Expo., 2018.
39. Cavalcanti MC, Bradaschia F, Neto MTD, Azevedo GMS, Cardoso TD. Dynamic modeling and control system design of the buck-boost-based threestate three-phase Z-source inverter. *Int J Electr Power Energy Syst*. Jan. 2019;104:654-663. https://doi.org/10.1016/j.ijepes.2018.07.034
40. Yalcin F, Three phase inverter based on buck-boost converter, Turkish Patent Institute, TR 2015 01839 B, filed 16.02.2015, applied 21.02.2018.
41. Kamal T, Arifoglu U, Hassan SZ. Buck-boost converter small signal model: dynamic analysis under system uncertainties. *J Electr Syst*. June 2018;14(2):165-178.

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