Real-time high-speed 5-D hyperchaotic Lorenz system on FPGA

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Abstract: Chaotic systems have several engineering applications such as cryptology, random number generators, image processing and secure communication. A basic structure used in these studies is a chaotic oscillator design that produces a chaotic signal. In this paper, 5-D hyperchaotic Lorenz system (Hu, 2009) has been implemented on FPGA using Heun algorithm to improve the chaos-based embedded engineering applications. The 32-bit IEEE-754-1985 floating point format has been used in the Heun-based design. The design has been coded in VHDL. The maximum operating frequency of FPGA-based 5-D hyperchaotic Lorenz system reaches 430.146 MHz. In addition, a real circuit realisation of 5-D hyperchaotic Lorenz system has been performed using analogue circuit elements. The results of FPGA-based new 5-D hyperchaotic Lorenz system have been compared with the results of computer-based numerical simulation and then the error analyses (MSE and RMSE) have been carried out.

Keywords: hyperchaos; FPGA; VHDL; Heun algorithm.

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1 Introduction

Hyperchaos is a non-linear phenomenon indicated by the presence of two or more Lyapunov characteristic exponents in non-linear systems of differential equations. Many hyperchaotic systems have been reported recently (Barboza, 2008; Jia, 2007; Gao et al., 2006; Jia et al., 2010; Zeng, 2011; Qi et al., 2008). Higher dimensional hyperchaotic systems of order $n \geq 5$ have been also proposed in the literature (Hu, 2009; Can and Uyaroglu, 2015; Kemih et al., 2015; Zarei, 2015). Modelling and computer implementation of systems are important topics in engineering and technology (Beddad et al., 2018; Xia et al., 2018; Vaidyanathan et al., 2018d; Tarkhaneh et al., 2018; Kumar and Khurana, 2018; Beddad et al., 2019).

Chaos theory featuring chaotic and hyperchaotic systems has applications in several branches of science and engineering such as oscillators (Vaidyanathan and Rasappan, 2011; Vaidyanathan, 2015h; Vaidyanathan, 2012a; Pakiriswamy and Vaidyanathan, 2012; Vaidyanathan, 2012b), robotics (Vaidyanathan et al., 2017; Celikovsky and Lynnyk, 2018), biology (Vaidyanathan et al., 2018f; Vaidyanathan, 2015f; Vaidyanathan, 2015b; Vaidyanathan, 2015c; Vaidyanathan, 2015e), ecology (Vaidyanathan, 2015g; Vaidyanathan, 2015a), mechanical systems (Vaidyanathan, 2015d; Chlouverakis and Sprott, 2006), steganography (Vaidyanathan et al., 2018a), weather systems (Vaidyanathan et al., 2018e; Vallis, 1986), neural networks (Vaidyanathan, 2015i; Wang and Lu, 2019; Lahmiri and Bekiros, 2019), encryption (Vaidyanathan et al., 2018b; Vaidyanathan et al., 2018c; Vaidyanathan and Rajagopal, 2017), secure communications (Wu et al., 2014; Li et al., 2005; Filali et al., 2014), finance (Tacha et al., 2016; Szuminski, 2018), circuits (Akgül et al., 2016b; Volos et al., 2015, 2017; Pham et al., 2016), etc.

Recently, the implementations related to the modelling of chaotic systems on FPGA has gained importance in Koyuncu et al. (2017), Rajagopal et al. (2017), Alcin et al. (2016), Tuna and Fidan (2016), Koyuncu et al. (2014), Lai et al. (2018), Koyuncu et al. (2013), Akgül et al. (2016a), Azzaz et al. (2013), Sadoudi et al. (2009), Tuna et al. (2018), Karthikeyan and Rajagopal (2018), Rajagopal et al. (2018), Koyuncu (2018) and Hua et al. (2018). Rajagopal et al. (2017) designed two new fractional-order 4D chaotic systems on Xilinx Kintex 7 FPGA chip using Matlab-Xilinx System Generator Toolbox. Alçin et al. (2016) proposed the design of Artificial Neural Networks (ANNs)-based Pehlivan-Uyaroglu Chaotic System (PUCS) using VHDL with IEEE-754 32-bit floating point arithmetic on Xilinx Virtex-6 FPGA chip. Tuna and Fidan (2016) accomplished the design of a new chaotic system using Heun algorithm on FPGA. This design has been coded in VHDL with IEEE-754 floating point number format (Tuna and Fidan, 2016). Koyuncu et al. (2014) proposed the design of Pehlivan-Wei Chaotic System (PWCS) using Euler, Heun and RK4 numerical algorithms on Virtex-6 FPGA chip in VHDL. Lai et al. (2018) designed the multi-butterfly chaotic system using VHDL on FPGA. Koyuncu et al. (2013) presented FPGA-based Burke-Shaw Chaotic System (BSCS) that uses RK5-Butcher (RK5B) numerical algorithm. The design has been created in VHDL with IEEE-754 floating point number standard on Virtex-6 chip (Koyuncu et al., 2013). Akgül et al. (2016a) accomplished the design of 3-D chaotic system using RK4 numerical algorithm on Xilinx FPGA chip. Table 1 presents the technical properties of the various FPGA-based chaotic oscillators implemented in recent years.

The organisational structure of this work is given as follows. Section 2 details the 5-D hyperchaotic Lorenz system derived by Hu (2009). Section 3 contains a detailed description and results of the real-circuit realisation of 5-D hyperchaotic Lorenz system (Hu, 2009). In Section 4, the 5-D hyperchaotic Lorenz system (Hu, 2009) has been implemented on FPGA using Heun algorithm in VHDL with 32-bit IEEE 754-1985 floating point number format. Additionally, the area utilisation report of the FPGA related to the chaotic system designed using Heun algorithm has been given. Mean Square Error (MSE) and Root Mean Square Error (RMSE) error analyses have been performed using the results obtained from both chaotic oscillator designs of the hyperchaotic Lorenz system. Finally, some concluding remarks are noted in the last section.

Table 1 The technical properties of the various FPGA-based chaotic oscillators implemented in recent years

References	*Chaotic system features*	*FPGA-based design*	*Oper. Freq. (MHz)*
Rajagopal et al. (2017)	4D Fractional order chaotic system	Xilinx system generator toolbox in Simulink	⋯
Alçin et al. (2016)	3D PU chaotic system	ANN, IEEE-754 32-bit floating-point	266.429
Tuna and Fidan (2016)	3D novel chaotic system	Heun, IEEE-754 32-bit floating-point	390
Koyuncu et al. (2014)	3D novel PW chaotic system	Euler, Heun, RK4, IEEE-754 32-bit floating-point	463.688
Lai et al. (2018)	4D multi-butterfly chaotic system	Xilinx System Generator toolbox in Simulink	⋯
Koyuncu et al. (2013)	3D Burke-Shaw chaotic system	RK5-Butcher, IEEE-754 32-bit floating-point	373.084
Akgül et al. (2016a, 2016b)	3D novel chaotic system	RK4, VHDL, IEEE 754-1985 32-bit floating-point	374.094
Tlelo-Cuautle et al. (2016)	50-scroll chaotic attractor	⋯	66
Azzaz et al. (2013)	3D hybrid chaotic system	Euler, IQ-Math fixed-point, 32-bit (16Q16)	38.860
Sadoudi et al. (2009)	Chen chaotic system	RK4, IEEE-754 32-bit floating-point	22.850
Hua et al. (2018)	Sine-transform-based chaotic system	IEEE-754 32- bit floating-point	22.850
This paper	5-D hyperchaotic Lorenz system	Heun numerical method, IEEE-754 32-bit floating-point	430.146

2 Five-dimensional hyperchaotic Lorenz system

This section gives a brief review of the 5-D hyperchaotic Lorenz system announced by Hu (2009).

Jia (2007) proposed a 4-D hyperchaotic system by extending the famous Lorenz chaotic system (Lorenz, 1963) as follows:

$$\begin{cases} \dot{x} = -\sigma(x-y)+w \\ \dot{y} = rx - y - xz \\ \dot{z} = xy - \beta z \\ \dot{w} = -xz + pw \end{cases} \tag{1}$$

In equation (1), x, y, z, w stand for the states and σ, r, β, p are positive constants.

In Jia (2007), the system (1) was shown to be hyperchaotic when $p = 1.3$ and $(\sigma, r, \beta) = \left(10, 28, \frac{8}{3}\right)$ as in Lorenz system (Lorenz, 1963).

For the initial state $X(0) = (0, -0.01, 9, 1)$ and $(\sigma, r, \beta, p) = \left(10, 28, \frac{8}{3}, 1\right)$, the Lyapunov exponents of the Jia system (1) are evaluated as

$$\begin{cases} \varphi_1 = 0.3618 \\ \varphi_2 = 0.2096 \\ \varphi_3 = 0 \\ \varphi_4 = -12.9371 \end{cases} \tag{2}$$

The presence of two positive Lyapunov exponents φ_1 and φ_2 in (2) pinpoints that the Jia system (1) is a 4-D hyperchaotic Lorenz system.

Hu (2009) proposed a 4-D hyperchaotic system from the Jia system (Jia, 2007) as follows:

$$\begin{cases} \dot{x} = -\sigma(x-y)+w \\ \dot{y} = rx - y - xz - v \\ \dot{z} = xy - \beta z \\ \dot{w} = -xz + pw \\ \dot{v} = qy \end{cases} \tag{3}$$

In equation (3), x, y, z, w, v stand for the state variables and σ, r, β, p, q are positive constants.

In Hu (2009), the system (3) was shown to be hyperchaotic when the parameter values are chosen as

$$\sigma = 10, \; r = 28, \; \beta = \frac{8}{3}, \; p = 2, \; q = 8 \tag{4}$$

For the initial state $X(0) = (0, -0.01, 9, 1, 0)$ and the constants as in (4), the Lyapunov exponents of the Hu system (3) are evaluated as

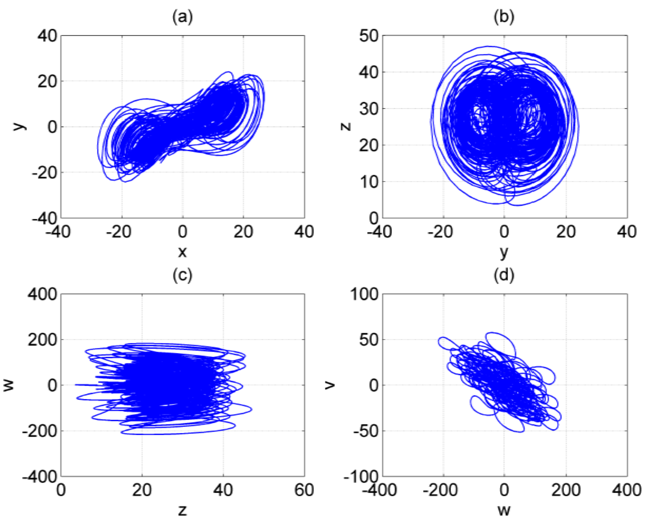
$$\begin{cases} \varphi_1 = 0.4895 \\ \varphi_2 = 0.3244 \\ \varphi_3 = 0.0554 \\ \varphi_4 = 0 \\ \varphi_5 = -12.5315 \end{cases} \tag{5}$$

The presence of three positive Lyapunov exponents φ_1, φ_2 and φ_3 in (5) pinpoints that the Hu system (3) is a 5-D hyperchaotic Lorenz system.

Figure 1 shows the 2-D projections of the Hu system (3) for $X(0) = (0, -0.091, 9, 1, 0)$ and $\left(\sigma, r, \beta, p, q\right) = \left(10, 28, \frac{8}{3}, 2, 8\right)$.

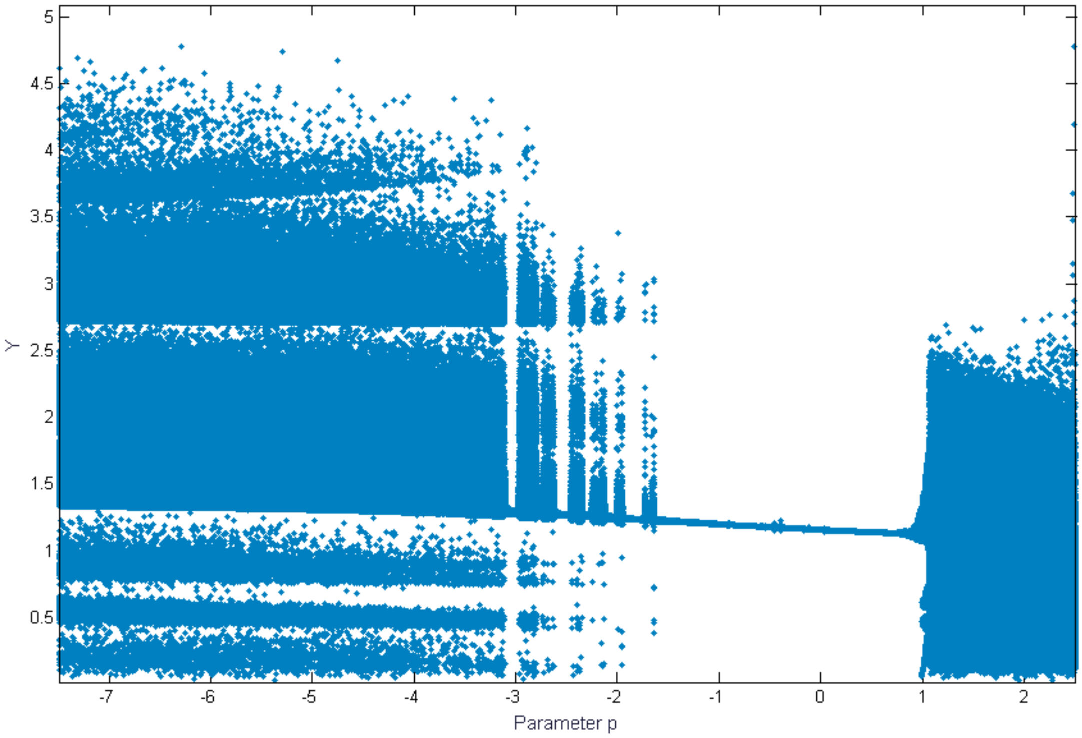
From Figure 1, it is seen that the Jia system (3, which is a 5-D hyperchaotic Lorenz system, exhibits a two-scroll attractor.

Figure 1 Two-dimensional projections of the hyperchaotic Lorenz system (3) for $X(0) = (0, -0.01, 9, 1, 0)$ and $\left(\sigma, r, \beta, p, q\right) = \left(10, 28, \frac{8}{3}, 2, 8\right)$



Next, we carry out a bifurcation analysis of the Hu system (3) by varying the parameter p between -7.5 and 2.5, and keeping the other parameters fixed. For this analysis, the initial states of the 5-D system (3) are taken as $x(0) = 0$, $y(0) = 0$, $z(0) = 0, 3.w(0) = 0$ and $v(0) = 0$. For a step size of 0.005, the bifurcation diagram in Figure 2 is obtained. As seen in Figure 2, hyperchaos is observed for $p < -3.1$ and $p > 1$.

Figure 2 The bifurcation diagram of the Hu system (3) for $X(0) = (0, 0, 0.3, 0, 0)$ by varying p in $[-7.5, 2.5]$, and keeping other parameters fixed as $(\sigma, r, \beta, q) = \left(10, 28, \frac{8}{3}, 8\right)$



3 Electronic circuit implementation of the 5-D hyperchaotic Lorenz system

The 5-D system (3) shows hyperchaotic oscillations when the parameters are chosen as $\sigma = 10,\ r = 28,\ \beta = 83,\ p = 2,\ q = 7.3$ and the initial conditions are taken as $X(0) = (0, 0, 0, 1, 1)$. The hyperchaotic system must be rescaled for electronic circuit implementation. The amplitude values of the states x, y, z, w, v are in the interval of $(-270, 230)$. They are higher than the interval of $(-15, 15)$ which are limitations of electronic materials.

For scale process, we let $X = x2.5,\ Y = y2,\ Z = z4,$ $W = w20$ and $V = v5$.

Then we adjust the original state variables x, y, z, w and v instead of the new variables X, Y, Z, W and V. Thus, the scaled system is obtained as follows:

$$\begin{cases} \dot{x} = -\sigma(x - y5) + 8w \\ \dot{y} = 54rx - y - 20xz - 5v4 \\ \dot{z} = -\beta z + 54xy \\ \dot{w} = -12xz + pw \\ \dot{v} = 25qy \end{cases} \tag{6}$$

An electronic circuit is defined for the scaled system (6) as shown in Figure 3.

The size of the circuit elements are $C1 = C2 = C3 = C4 = C5 = 1nF$, $R1 = R3 = 50\ k\Omega$, $R2 = 40\ k\Omega$, $R5 = 8\ k\Omega$, $R6 = 159.68\ k\Omega$, $R7 = 11.4\ k\Omega$, $R8 = 32\ k\Omega$, $R9 = 149.698\ k\Omega$, $R10 = 80\ k\Omega$, $R11 = 200\ k\Omega$, $R12 = 136.7\ k\Omega$, $R13 = R14 = R15 = R16 = R17 = R18 = R19 = R20 = R21 = R22 = 100\ k\Omega$.

The phase-portraits on the oscilloscope for the 5-D hyperchaotic Lorenz system are shown in Figure 4. Also, the scaled hyperchaotic system is physically realised on the electronic card shown in Figure 5.

Figure 3 Electronic circuit scheme of the 5-D hyperchaotic Lorenz system (6)

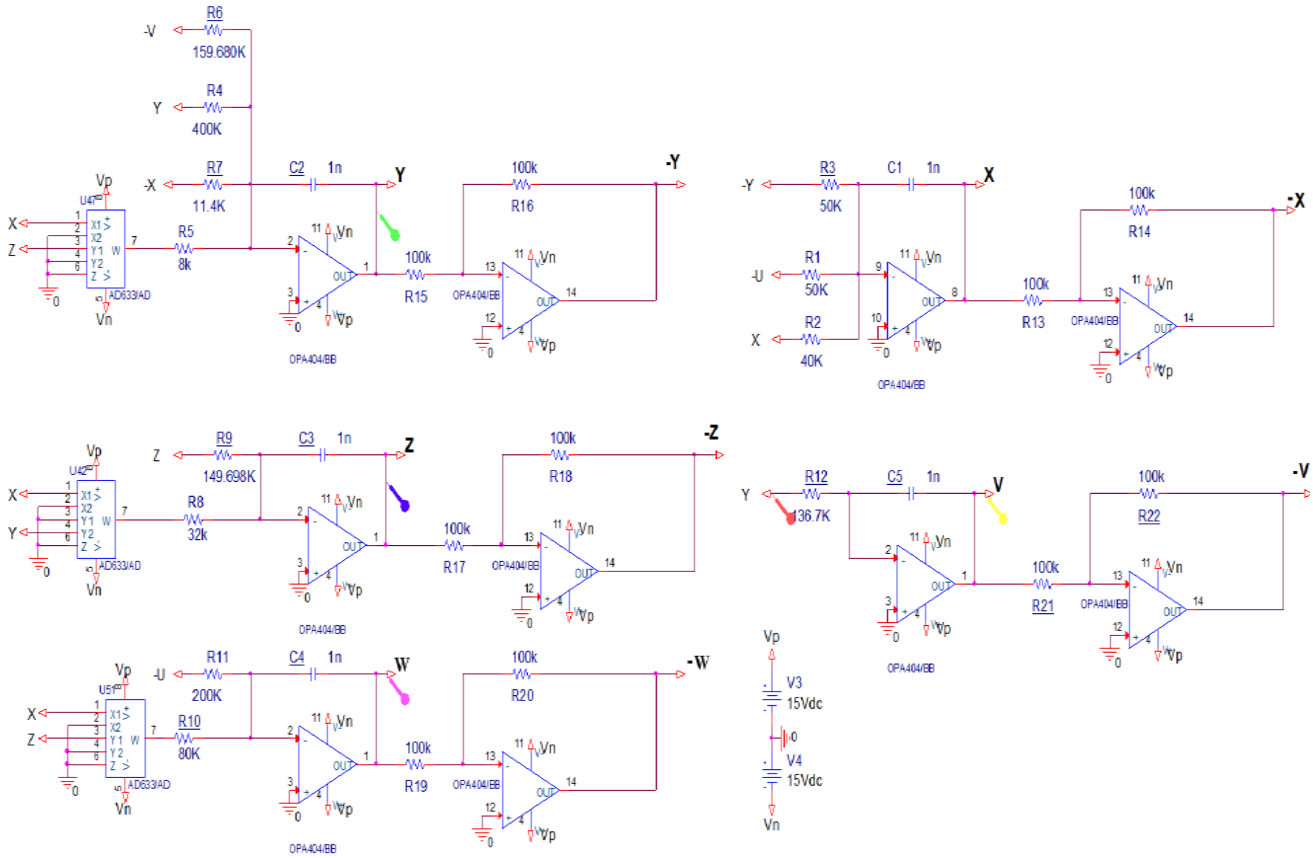
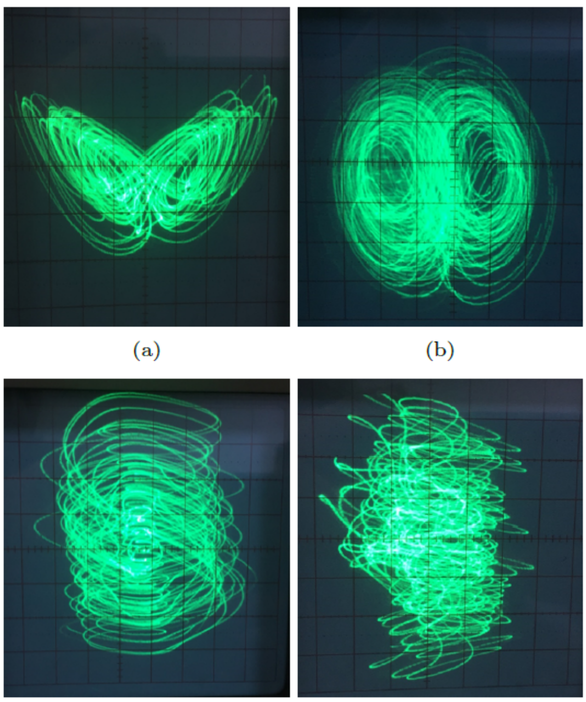


Figure 4 The phase plots of the 5-D hyperchaotic Lorenz system (6) on the oscilloscope



(a) (b)

(c) (d)

Figure 5 Real-circuit design of the 5-D hyperchaotic Lorenz system (6)

4 FPGA-based 5-D hyperchaotic Lorenz system

In this section, the 5-D hyperchaotic Lorenz system (Hu, 2009) has been modelled using Heun algorithm in VHDL as a Hardware Description Language (HDL) with 32-bit IEEE 754-1985 floating point number format on

FPGA. The units such as multiplier, adder and subtractor, which have been utilised in the construction of the designs of units and have been compatible with fixed point number standard, have been created using IP-Core Generator that produced by Xilinx ISE Design Tools. The mathematical expression related to Heun algorithm is given in equation (7).

$$\begin{cases} y(x_0) = y_i = y_0 \\ y^0_{\lambda+1} = y_\lambda + f(y_\lambda)\cdot\Delta h \\ y_{\lambda+1} = y_\lambda + f(y_\lambda) + y^0_{\lambda+1} 2\cdot\Delta h \end{cases} \tag{7}$$

In equation (7), y_0 and Δh represent the initial conditions of the 5-D hyperchaotic Lorenz system (3) and the step-size of the numerical method, respectively.

The Heun algorithm has two stages, which are described as follows. In the first stage, the value of $f\left(y^0_{\lambda+1}\right)$ has been calculated. In the second stage, the next iterate of the system $f\left(y_{\lambda+1}\right)$ has been calculated using the values of $f\left(y^0_{\lambda+1}\right)$ and y_λ.

$$\begin{cases} x^0(k+1) = x(k) + \left[-\sigma\left(x(k) - y(k)\right) + w(k)\right]\Delta h \\ x(k+1) = x(k) + \frac{1}{2}\left[-\sigma\left(x(k) - y(k)\right) \right. \\ \qquad \left. + w(k) + x^0(k+1)\right]\Delta h \end{cases} \tag{8}$$

$$\begin{cases} y^0(k+1) = y(k) + \left[rx(k) - y(k) - x(k)z(k) - v(k)\right]\Delta h \\ y(k+1) = y(k) + \frac{1}{2}\left[rx(k) - y(k) - x(k)z(k) \right. \\ \qquad \left. - v(k) + y^0(k+1)\right]\Delta h \end{cases} \tag{9}$$

$$\begin{cases} z(k^0+1) = z(k) + \left[-\beta z(k) + x(k)y(k)\right]\cdot\Delta h \\ z(k+1) = z(k) + \frac{1}{2}\left[-\beta z(k) \right. \\ \qquad \left. + x(k)y(k) + z^0(k+1)\right]\cdot\Delta h \end{cases} \tag{10}$$

$$\begin{cases} w^0(k+1) = w(k) + \left[-x(k)z(k) + pw(k)\right]\cdot\Delta h \\ w(k+1) = w(k) + \frac{1}{2}\left[-x(k)z(k) \right. \\ \qquad \left. + pw(k) + w^0(k+1)\right]\cdot\Delta h \end{cases} \tag{11}$$

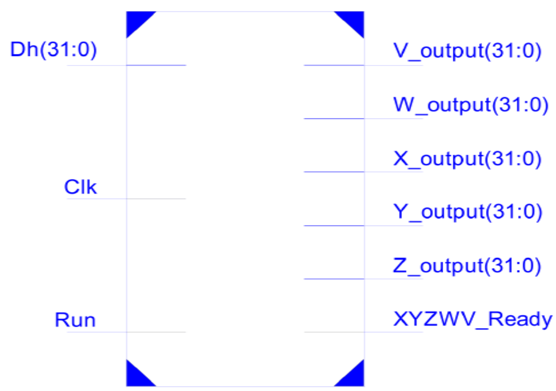
$$\begin{cases} v^0(k+1) = v(k) + qy(k)\Delta h \\ v(k+1) = v(k) + \frac{1}{2}\left[qy(k) + v^0(k+1)\right]\Delta h \end{cases} \tag{12}$$

Heun-based discretised mathematical model of the 5-D hyperchaotic Lorenz system is given in equations (8)–(12). In this set of equations, $x^0(k+1)$, $y^0(k+1)$, $z^0(k+1)$, $w^0(k+1)$ and $v^0(k+1)$ have been calculated using the values of $x(k), y(k), z(k), w(k)$ and $v(k)$.

Then $x(k+1)$, $y(k+1)$, $z(k+1)$, $w(k+1)$ and $v(k+1)$ values of the difference equation have been found for the first values when the step-size is incremented with the value of Δh. For the modelling of the 5-D hyperchaotic Lorenz system, we have chosen the step-size of the numerical Heun algorithm as $\Delta h = 0.005$.

For the FPGA-based modelling of the 5-D hyperchaotic Lorenz system using Heun algorithm, VHDL has been employed as a HDL. The top level block diagram of the designed FPGA-based oscillator has been illustrated in Figure 6. *Start* and *Clk* are one bit signals and located at the inputs of the unit. These signals are responsible for timing of all units and synchronising between units and their related system. To provide more flexible design, the step size Δh of the 5-D hyperchaotic Lorenz system has been applied from outside. The initial values that are necessary for the system startup have been embedded into the design using four different signals each have 32 bit for reducing the resource utilisation of FPGA chip employed in the design. However, as it is required, there is possibility to design the system to set the initial values by making slight changes in the system. In the designed Heun-based hyperchaotic oscillator unit, there are five 32-bit output signals (X_out, Y_out, Z_out, W_out and V_out) each have compatibility with floating point number standard and one bit XYZWV_Ready signal to demonstrate whether the output signals are ready.

Figure 6 The top-level block diagram of the designed FPGA-based hyperchaotic oscillator



The level 2 block diagram of the 5-D hyperchaotic Lorenz system is demonstrated in Figure 7. Chaotic signal generator includes three blocks. These blocks can be listed as (1) *MUX*, (2) *5D_Chaotic_Oscillator* and (3) *Filter*.

Figure 7 The level 2 block diagram of FPGA-based 5-D hyperchaotic Lorenz system

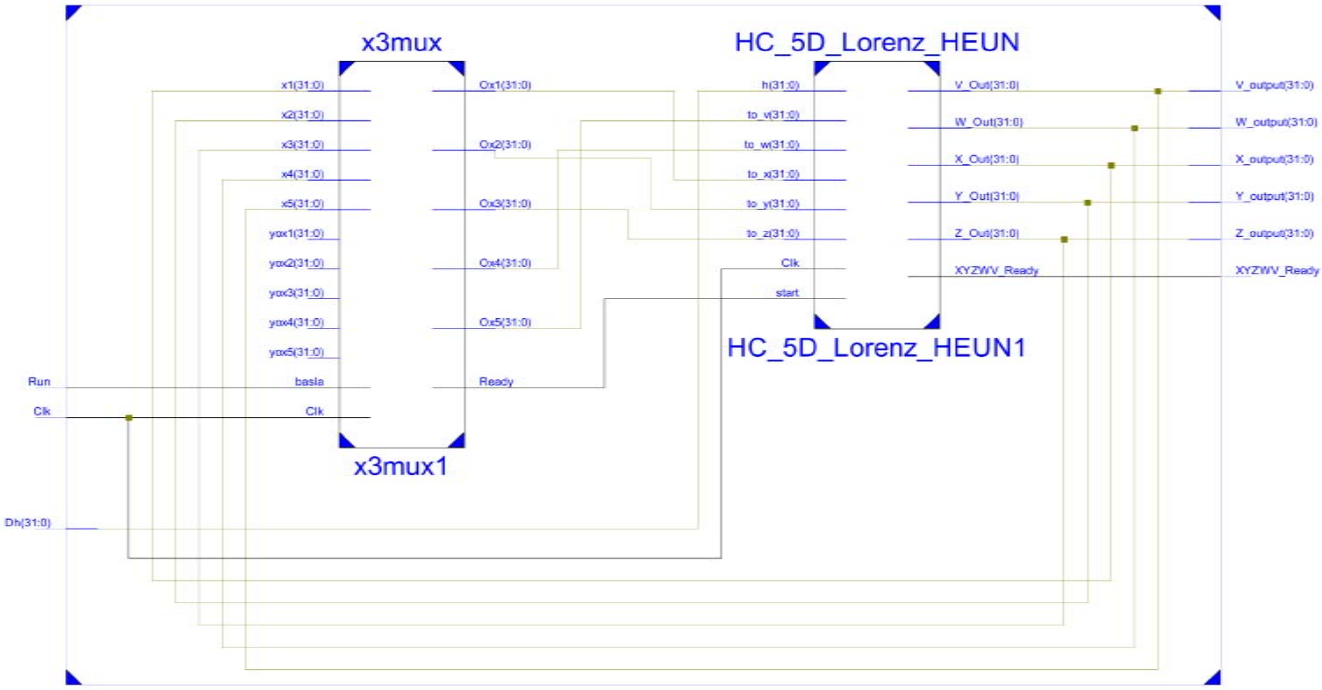
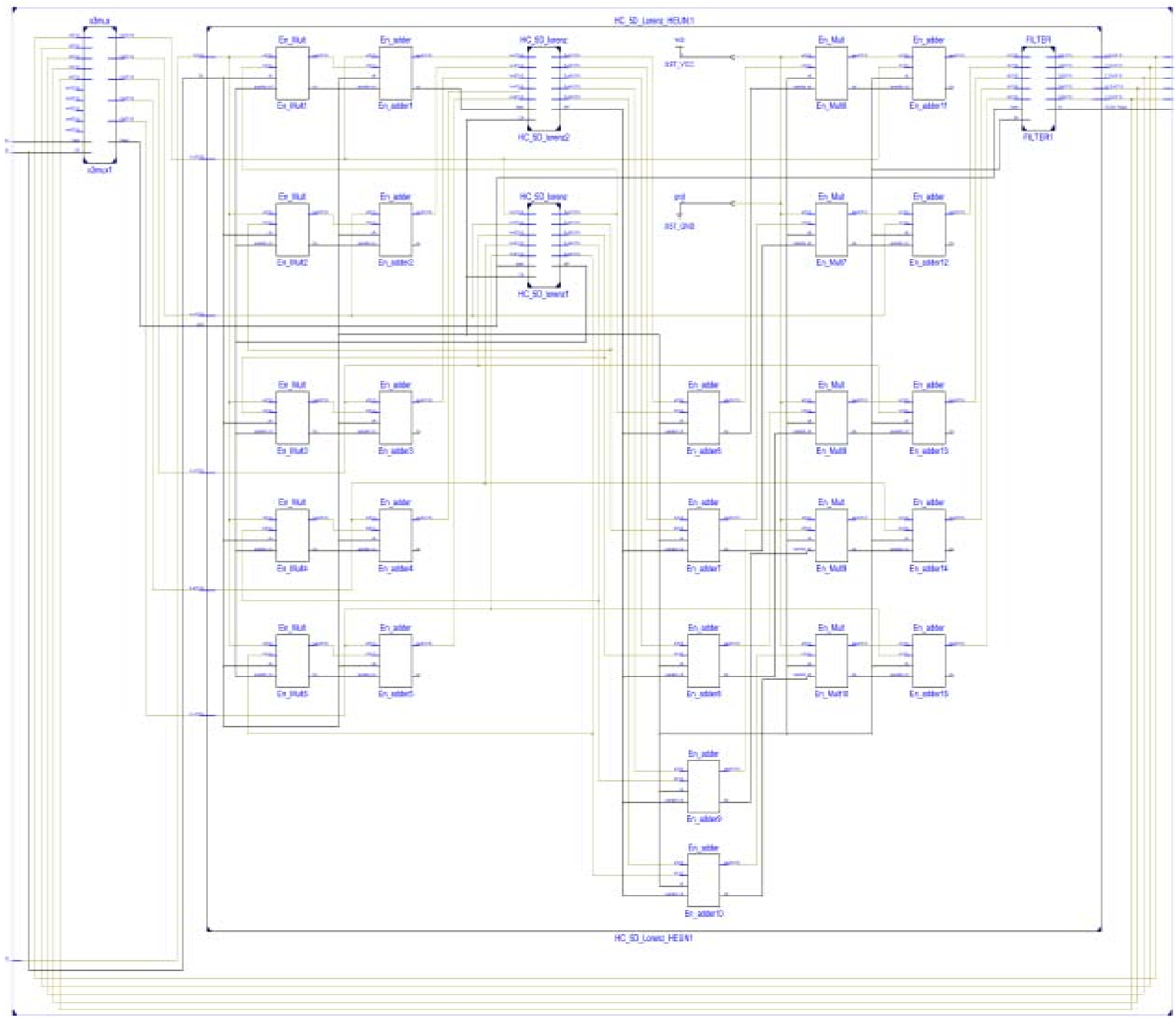


Figure 8 The level 3 block diagram of Heun-based 5-D hyperchaotic Lorenz System



Block 1 is the MUX unit that gives the initial state of the system. Block 2 is the *5D_Chaotic_Oscillator* unit that yields chaotic signals. Block 3 is the *Filter unit* used for preventing *5D_Chaotic_Oscillator* from producing unwanted signals. When the Run signal is active in the system, the values of initial state will be assigned from the values that have been defined in the chaotic signal generator.

When the chaotic oscillator yields the first values, *XYZWV_Ready* will take the value 1. Afterwards, the chaotic signal generator takes the values of the initial state from the chaotic signals that are produced at its output.

There are five signals each having 32-bit floating point standard namely, *X_output*, *Y_output*, *Z_output*, *W_output*, *V_output* and a control signal namely *XYZWV_Ready*, that shows these five signals being transferred to the output of the designed system. The signals originated from the filter unit form not only the outputs of the system but also the iterative values $x(k+1)$, $y(k+1)$, $z(k+1)$, $w(k+1)$ and $v(k+1)$ that are used as the values of initial state by transferring to *MUX unit*.

The level 3 block diagram of Heun-based 5-D hyperchaotic Lorenz oscillator unit has been illustrated in Figure 8. The *oscillator unit* includes eight units namely, *MUX*, f^0, *Multiplier*, *Divider*, *Adder* and f *units*. f^0 *unit* is responsible for determining the signals emerging from MUX unit and the state values $x(k+1), y(k+1), z(k+1), w(k+1)$ and $v(k+1)$ in the equations of the 5-D hyperchaotic Lorenz system.

The signals derived from f^0 *unit* have been multiplied with Δh using *Multiplier unit* and then the results have been summed with the initial state values of the hyperchaotic oscillator $x(k)$, $y(k), z(k), w(k)$, and $v(k)$. In this manner, the first stage of the algorithm has been completed.

In Stage 2 of the algorithm, the signals obtained from *Adder unit* have been added with the signals emerging from f^0 unit and then the results have been divided by 2.0 value which is the floating point number format (FP-2) using *divider unit*. The output signals of the *divider unit* have been added with the previously produced signals $(x(k), y(k), z(k), w(k)$, and $v(k))$ of the *chaotic oscillator unit* using *Adder unit* and then the obtained results have been sent to *Filter unit*.

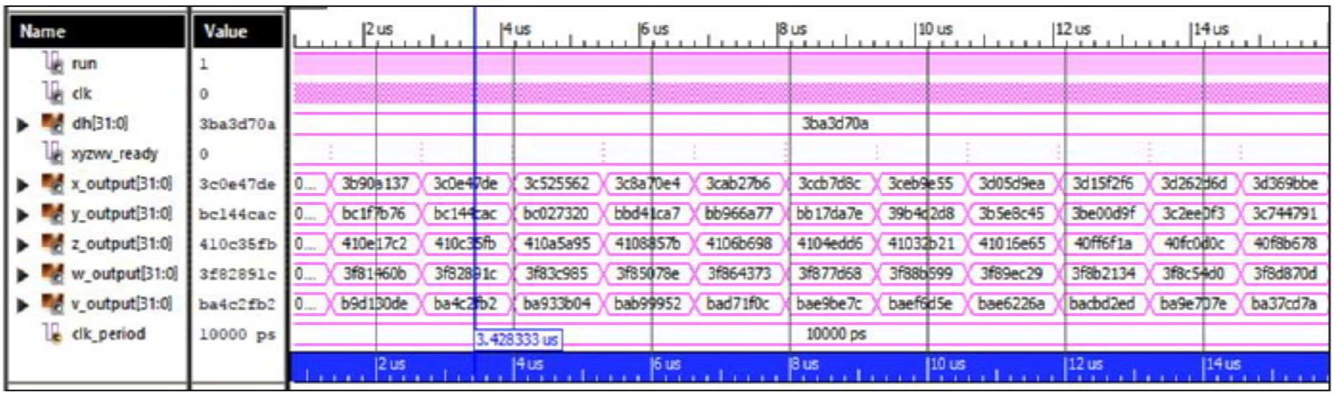
Multiplier, *Adder*, *Subtractor* and other units having 32 bit floating point number format in the Heun-based systems, have been generated with the IP Core Generator which is made by Xilinx. The system runs in pipelined manner and yields the first outputs after 132 clock cycles. The implemented chaotic signal generator has been simulated and synthesised for the *Xilinx Virtex6* (*xc6vlx75t-3ff784*) FPGA chip. Xilinx ISE numerical simulation results derived from the execution of the Heun-algorithm for the 5-D hyperchaotic Lorenz chaotic generator have been given in Figure 9.

The implementation of the 5-D hyperchaotic Lorenz system on FPGA using Heun numerical algorithm has been carried out and chip statistics have been obtained. The 5-D hyperchaotic Lorenz system has been designed compatible with VHDL IEEE 754-1985 floating point number standard on FPGA and as a result the maximum operating frequency of FPGA-based 5-D hyperchaotic Lorenz system reaches 430.146 MHz. After the Place and Route process, the chip statistics have been obtained and summarised in Table 2. Measured minimum time period of the designed unit is 2.325 ns.

Table 2 Hardware utilisation statistics (Xilinx Virtex-6 xc6vlx75t-3ff784 chip) of the 5-D hyperchaotic Lorenz system modelled by Heun-based algorithm

Logic utilisation	*Used*	*Available*	*Utilisation (%)*
No. of slice registers	28,669	93,120	30
No. of occupied slices	8,373	11,640	71
No. of bonded IOBs	195	360	54
No. of slice LUTs	28,6723	46,560	61
No. of BUFG/ BUFGCTRLs	1	32	3

Figure 9 Xilinx ISE simulation results obtained by the Heun-based 5-D hyperchaotic Lorenz chaotic oscillator unit



Lastly, the signals, namely *X_output*, *Y_output*, *Z_output*, *W_output* and *V_output* derived from the FPGA execution of Heun-based 5-D hyperchaotic Lorenz system have been saved in a file in 32-bit IEEE 754-1985 floating point number format during the test phase. After the conversion of saved values to real-number system, time series and phase portraits of the output signals have been obtained using the produced 5 × 3500 data set by the chaotic oscillator. The time series of *x*, *y*, *z*, *w* and *v* related to Heun-based 5-D hyperchaotic Lorenz system have been given in Figure 10.

The 2-D phase plots ($x - y, x - z, y - z, x - w, y - v$ and *w–y*) of the 5-D hyperchaotic Lorenz system modelled by discrete-time using Heun algorithm on FPGA have been illustrated in Figure 11.

Figure 10 The time series of $x(t)$, $y(t)$, $z(t)$, $w(t)$ and $v(t)$ related to Heun-based 5-D hyperchaotic Lorenz system implemented (a) in Matlab and (b) on FPGA

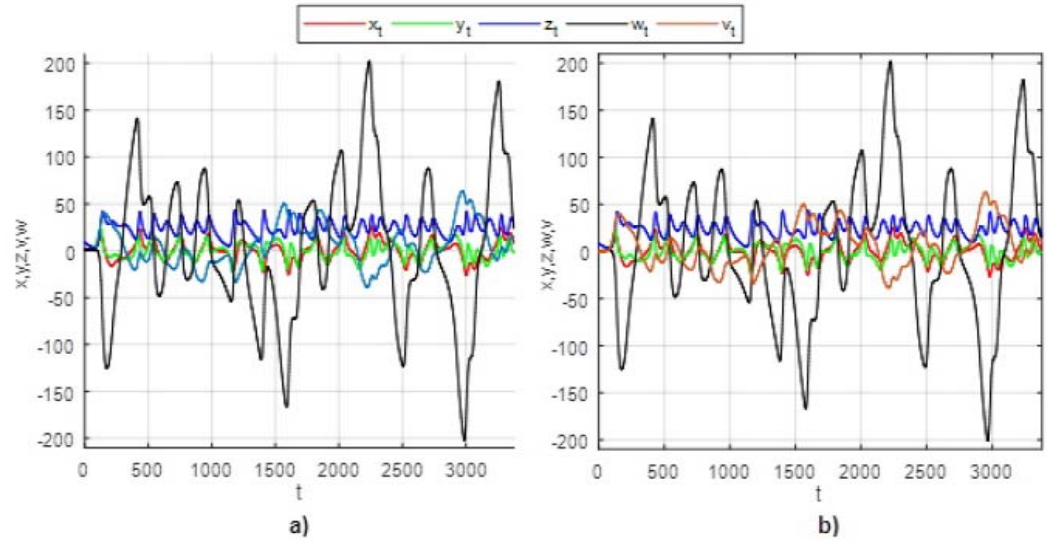


Figure 11 The 2-D phase portraits ($x - y$, $x - z$, $y - z$, $x - w$, $y - v$ and $w - v$) of the discrete-time 5-D hyperchaotic Lorenz system modelled using Heun algorithm on FPGA

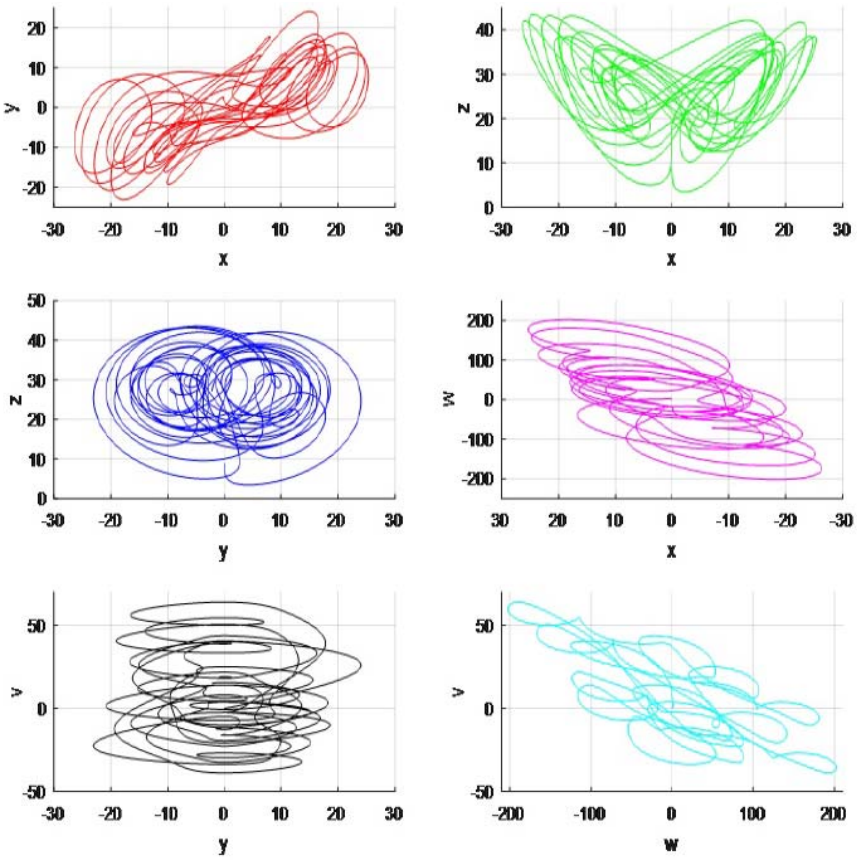
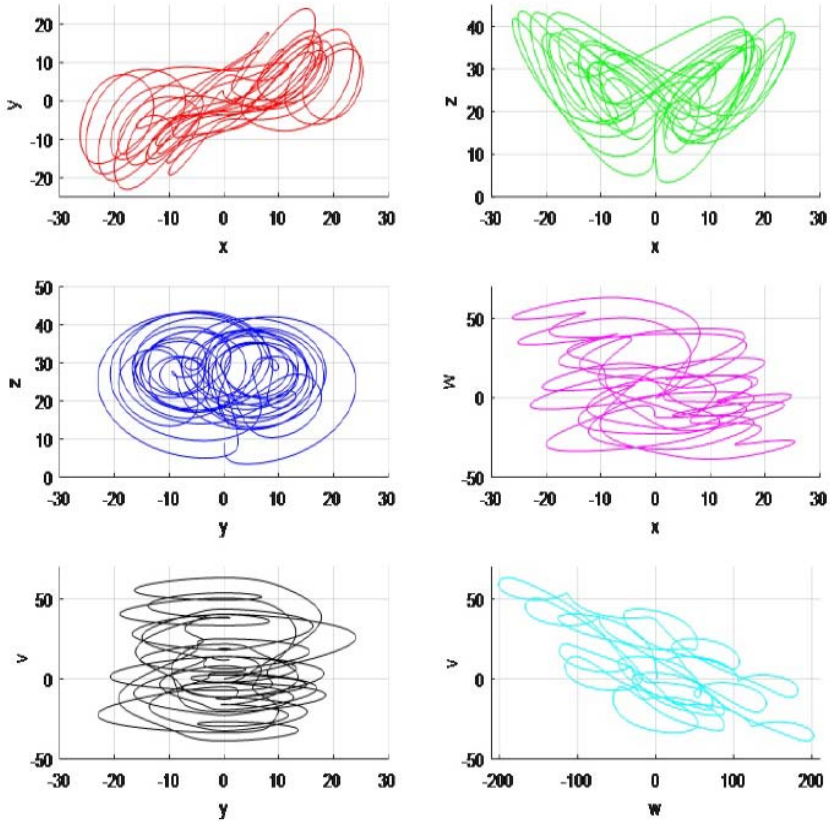


Figure 12 The 2-D phase portraits ($x-y$, $x-z$, $y-z$, $x-w$, $y-v$ and $w-v$) of the numerical-based 5-D hyperchaotic Lorenz system modelled using Heun algorithm in MATLAB



Also, the two-dimensional phase plots ($x-y, x-z, y-z, x-w, y-v$ and $w-v$) of the 5-D hyperchaotic Lorenz system modelled by the numerical-based Heun algorithm in MATLAB are shown in Figure 12.

Furthermore, the results of FPGA-based model have been compared with the results of Heun-based model. Hence, the error analyses of these methods namely, their MSE and RMSE values have been utilised for validation using equations (13) and (14). Table 3 presents the MSE and RMSE values of x, y, z, w and v .

Table 3 The MSE and RMSE results of 5 × 1000 values produced using MATLAB-based and FPGA-based Hyperchaotic Lorenz oscillator

State	*MSE*	*RMSE*
x	0.548694301	0.740739023
y	0.740812347	0.860704564
z	0.940663384	0.969878026
w	1.03700163	1.075372380
v	0.617673926	0.785922341

$$MSE = 1n \sum_{i=1}^{n} \left(x_i - \hat{x}_i \right)^2 \quad (13)$$

$$RMSE = \sqrt{1n \sum_{i=1}^{n} \left(x_i - \hat{x}_i \right)^2} \quad (14)$$

Parameters x_i , $\hat{x}_i$ and n denote the calculated value of Heun numerical algorithm-based computer model, the produced value of FPGA-based hardware model and the sample number used for evaluation, respectively. As a result, it has been observed that the MSE and RMSE values were quite low with respect to the produced results of the FPGA-based 5-D hyperchaotic Lorenz oscillator model designed in VHDL 32-bit IQ-Math fixed-point format using Heun-algorithm.

5 Conclusion

In this study, FPGA-based discrete-time implementation of the 5-D hyperchaotic Lorenz system (Hu, 2009) has been performed. In the design, the Heun numerical algorithm has been used. The design has been coded in VHDL language using 32-bit IEEE 754–1985 floating point number standart. The maximum operating frequency of the designed unit reaches 430.146 MHz. It is observed that there has been strong convergence between the phase portraits obtained from computer-based numerical analysis, analogue circuit design and FPGA-based design with respect to the results of the study. As a result, the results produced by the chaotic oscillator designed on Matlab and FPGA have been analysed and therefore MSE and RMSE have been evaluated for 1000 data sets. The results of the proposed FPGA-based unit converge successfully to the results of the Matlab-based numeric model. The successful results obtained from the design of 5-D hyperchaotic Lorenz system on FPGA have shown that this hyperchaotic system can be utilised in embedded hyperchaos-based engineering applications such as cryptosystems, random number generators, image processing and secure communication. In future, various applications including data masking, synchronisation and steganography can be carried out with the discrete-time implemented 5-D hyperchaotic Lorenz system on FPGA.

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