






## Research Article

# Active Realization of Fractional-Order Integrators and Their Application in Multiscroll Chaotic Systems

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Received 2 October 2020; Revised 29 December 2020; Accepted 4 January 2021; Published 20 January 2021

Academic Editor: Carlos Aguilar-Ibanez

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This paper presents the design, simulation, and experimental verification of the fractional-order multiscroll Lü chaotic system. We base them on op-amp-based approximations of fractional-order integrators and saturated series of nonlinear functions. The integrators are first-order active realizations tuned to reduce the inaccuracy of the frequency response. By an exponential curve fitting, we got a convenient design equation for realizing fractional-order integrators of orders from 0.1 to 0.95. The results include simulations in SPICE of the mathematical description and the electronic implementation and experimental measurements that confirm them. Monte Carlo and sensitivity tests revealed a robust realization. Contrary to its passive counterparts, the suggested realizations significantly reduce design and implementation efforts by favoring resistors and capacitors with commercial values and reducing hardware requirements.

## 1. Introduction

Fractional calculus has been known since 1695 when L'Hôpital and Leibniz interchange letters about the non-integer order of the derivative. The fractional calculus is considered as a generalization of the integer-order version. Fractional-order derivatives are characterized by their memory properties providing an excellent approach for describing the physical phenomena elegantly with improved accuracy [1, 2]. As a result, the researchers have proposed novel mathematical models with applications in various fields, such as biology, economics, chaos theory, botany,

hidden dynamics, digital circuits, cryptography, control, image processing, wind turbines, viscoelastic studies, and ferroelectric materials [3–15].

Regarding chaos, there has been recently an increased number of works reporting fractional-order chaotic systems because fractional order provides an extra degree of freedom, which can be useful for generating diverse dynamics such as self-excited attractors, hidden attractors, multistability, and extreme stability [16–20]. In particular, the multiscroll chaotic attractors present plenty of complex topological structures contrary to single- or double-scroll attractors. One of the most typical applications is secure

communications, e.g., in random number generators, cryptosystems in wireless networks, and image encryption [21–23]. Therefore, it is a subject of increasing interest [24–30].

The physical realization of chaotic systems is a well-accepted technique to observe the chaotic behaviors and therefore validates the theoretical findings. From an engineering point of view, the challenge consists of implementing the fractional-order multiscroll chaotic systems physically since there is not a fabricated fractional-order capacitor yet commercially available [31, 32]. Hence, in the literature, we can find two approaches for implementing fractional-order differential equations that describe the chaotic systems. On the one side, the embedded methodology uses FPGAs or DSPs to describe the fractional-order dynamical system by implementing a numerical method to solve computationally the system rather than an electronic circuit [33]. Nevertheless, this approach has been demonstrated that induces degradation effects corrupting the chaos generation. On the other side, the analog method employs essential circuit elements for obtaining the fractional-order integrators. The basic idea consists of representing the fractional order with an integer-order transfer function of high degree. As a result, the electronic realization of the fractional integrator depends on a tree-like passive network formed with resistors and capacitors. However, the resulting passive emulator circuits nor contain commercial values neither a suitable design equation between elements (ratio of values), provoking a complexity for a proper tuning of the fractional order for observing chaos behavior. Therefore, the works focused on the physical implementation of fractional-order chaotic systems generating multiscrolls are limited and only found with implementations using passive networks [24–28].

The question arising is how to obtain a straightforward approach for implementing fractional-order multiscroll chaotic systems with analog topologies? This paper will give a positive answer to this question. A first response is to use fractional-order integrators derived from an active circuit topology, which can be designed with circuit elements of commercial values or using an appropriate ratio of values. In this regard, some first results were proposed in refs. [31, 32], which reported active realization using integrated circuit technology. However, that approach has not been proved in either single-scroll or multiscroll chaotic systems. Therefore, the main contributions of this paper are as follows: (i) an optimized design methodology is proposed based on continued fraction expansion to obtain an active fractional integrator which can be related in a quick way to the fractional order of the chaotic systems; (ii) to the best knowledge of authors, the first experimental validation of a fractional-order multiscroll chaotic system is proposed based on active circuit topologies; and (iii) additionally, we perform an exhaustive study to demonstrate that the proposed design methodology is robust to statistical variations of element values and insensible to changes in the circuit elements.

The electrical circuits to realize fractional-order integrators are based on “fractances,” electrical elements with

fractional-order impedance. These elements produce a magnitude frequency response with roll-off  $\pm 20\alpha$  dB/dec and constant-phase response of  $\pm 90\alpha$  degrees [34]. Unfortunately, the nonexistence of circuit elements with fractional response challenges carries out fractional-order transfer functions. The alternative is the approaching of fractances in a desired bandwidth with rational functions by means of methods of approximation such as Muir, Matsuda, Newton, Carlson, Oustaloup, power series (PSE), and continuous fraction expansion (CFE) [34–36]. The larger the order of the approximation, the larger the bandwidth where it is valid. Once got the rational function, the synthesis is possible using ladder networks of Cauer or Foster [36], tree structures, or transmission lines [35, 36]. The disadvantage of these realizations is the difficulty to approximate the required elements with commercially available resistances, capacitors, inductors, and even negative impedance converters, which results in bulky realizations [36–39]. For instance, Figure 1 shows a third-order realization using the Charef approach for a fractional-order passive fractance with  $\alpha = 0.95$ , an error of 1 dB, and a bandwidth from 0.1 rad/s to 1000 rad/s [40]. The circuit requires three resistors and three capacitors of disperse and not available values. To avoid this drawback in this paper, we present two proposals of implementation of  $s^{-\alpha}$  with active elements based on algebraic manipulation of a first-order CFE approximation. Despite its inaccuracy, in this work, we explore the use of a compact first-order approximation with  $\alpha \in (0, 1)$  obtained by the CFE approach, but tuned to reduce error in the magnitude’s slope response. It has the form [34]

$$\frac{1}{s^\alpha} \approx \frac{(1-\alpha)s + (1+\alpha)}{(1+\alpha)s + (1-\alpha)} = \frac{s+A}{As+1},$$

$$A = \frac{1+\alpha}{1-\alpha}. \quad (1)$$

This article is organized as follows. Section 2 provides a brief survey of fractional calculus, approximation of fractances, and op-amp-based building blocks. Section 3 depicts the circuit realization of the fractional-order integrator and presents Monte Carlo and sensitivity tests. Section 4 offers simulation and experimental results of the Lü chaotic oscillator and discusses the advantages of the proposed realization. We draw the conclusion in Section 5.

## 2. Theoretical Background

This section describes theoretical background such as fractional-order calculus, the Laplace transform of a fractional derivative, and op-amp-based building blocks for implementing fractional-order integrators and chaotic oscillators.

*2.1. Fractional Derivative and Fractional Laplacian Operator.* The Riemann–Liouville definition for calculation of fractional derivatives and integrals of a function  $f(t)$  establishes [41, 42]

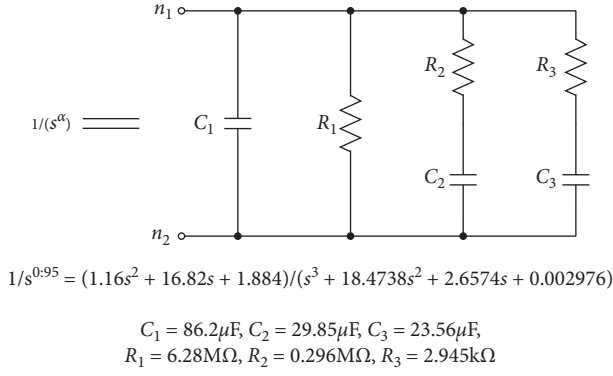


FIGURE 1: Approximation of a fractional-order passive fractance with  $\alpha = 0.95$  and error of 1 dB.

$$\mathcal{D}_t^\alpha f(t) = \frac{1}{\Gamma(m-\alpha)} \left( \frac{d}{dt} \right)^m \int_0^t \frac{f(\tau) d\tau}{(t-\tau)^{\alpha-m+1}}, \quad (2)$$

where  $\alpha \in \mathbb{R}$  is the fractional order,  $m-1 < \alpha < m$ ,  $m \in \mathbb{N}$ , and  $\Gamma(\cdot)$  is the gamma function. For  $\alpha > 0$ ,  $\alpha < 0$ , and  $\alpha = 0$ , one gets the fractional derivative, fractional integral, and identity function. The Laplace transform of (2) with zero initial conditions becomes [41]

$$\mathcal{L}\{\mathcal{D}_t^\alpha f(t)\} = s^\alpha F(s), \quad (3)$$

where  $F(s)$  stands for Laplace transform of  $f(t)$  and  $s^\alpha$  is the fractional Laplacian operator given by

$$s^\alpha = (j\omega)^\alpha = \omega^\alpha \left[ \cos\left(\frac{\alpha\pi}{2}\right) + j \sin\left(\frac{\alpha\pi}{2}\right) \right]. \quad (4)$$

**2.2. Op-Amp-Based Building Blocks.** The circuits of Figure 2 are the analog electronic blocks used in this paper to realize fractional-order integrators and chaotic oscillators. The selection of  $R_g$ ,  $R_s$ ,  $R_y$ ,  $C_x$ , and  $\Omega$  as degrees of freedom will allow reducing the number of passive elements with disperse or not commercially available values.

**2.2.1. Weighted Differential Amplifier (WDA).** The op-amp-based amplifier of Figure 2(a) amplifies the weighted difference between two voltages  $V_{1A}$  and  $V_{2A}$  with pondering factors depending on  $R_{g1}$  and  $R_{g2}$ . By nodal analysis, the output voltage  $V_{\text{out},A}$  can be calculated as

$$V_{\text{out},A} = \frac{R_g}{R_{g1}} V_{1A} - \frac{R_g}{R_{g2}} V_{2A}. \quad (5)$$

**2.2.2. Weighted Adder Amplifier (WAA).** The amplifier of Figure 2(b) provides the weighted sum of two voltages  $V_{1B}$  and  $V_{2B}$  given by

$$V_{\text{out},B} = \frac{R_g}{R_{h1}} V_{1B} + \frac{R_g}{R_{h2}} V_{2B}, \quad (6)$$

where  $R_{h1}$  and  $R_{h2}$  control the pondering factors. Note that since this circuit is a noninverter adder based on a voltage series feedback amplifier, it presents a negative feedback loop which adds up stability to the weighted coefficients of  $V_{1B}$  and  $V_{2B}$ , which in turn are the pondering factors  $(R_g/R_{h1})$  and  $(R_g/R_{h2})$ .

**2.2.3. Inverting Integrator (Innv).** The circuit of Figure 2(c) uses capacitive feedback to integrate the voltage  $V_{1C}$  through

$$\frac{V_{\text{out},C}}{V_{1C}} = -\frac{1}{R_x C_x s} = -\frac{1}{s},$$

$$R_x = \frac{1}{C_x}. \quad (7)$$

A capacitor  $C$  can replace  $C_x$  to translate the frequency response by a factor  $\Omega$ , where

$$C = \frac{C_x}{\Omega}. \quad (8)$$

In the time domain, expression (7) is rearranged to be written as

$$V_{\text{out},C} = -\frac{1}{R_x C_x} \int_0^t V_{1C} dt. \quad (9)$$

**2.2.4. Inverting Amplifier (Inv).** The circuit of Figure 2(d) provides a negative voltage gain given by

$$\frac{V_{\text{out},D}}{V_{1D}} = -\frac{R_b}{R_a}. \quad (10)$$

This negative gain is indicative of an inverting amplifier with a  $180^\circ$  phase shift between  $V_{1D}$  and  $V_{\text{out},D}$ . The gain can be greater than, less than, or equal to 1 depending on the values of  $R_a$  and  $R_b$ .

**2.2.5. Inverting Weighted Adder Amplifier (IWAA).** The amplifier of Figure 2(e) provides a weighted negative sum of four input voltages  $V_{1E}$ ,  $V_{2E}$ ,  $V_{3E}$ , and  $V_{4E}$  with pondering factors  $a$ ,  $b$ ,  $c$ , and  $d$ . By nodal analysis, the output voltage  $V_{\text{out},E}$  can be calculated as

$$V_{\text{out},E} = aV_{1E} + bV_{2E} + cV_{3E} + dV_{4E}. \quad (11)$$

**2.2.6. PWL Function Emulator (PWL).** Multiscroll chaotic oscillator circuits use saturated nonlinear functions (SNLFs) approximated by piecewise linear (PWL) functions [43, 44]. Figure 2(f) shows the SNLF for generating two and four scrolls. The number of scrolls achieved is the number of saturated levels, in this case with amplitudes  $E_1$ ,  $E_2$ ,  $E_3$ , and  $E_4$ . The breakpoints of the SNLF are  $e_1$ ,  $e_2$ , and  $e_3$ . Figure 2(g) represents the corresponding electronic realization. To generate two scrolls, the circuit requires two op-amps with two saturated levels at  $E_1$  and  $E_2$  and a shifted voltage (breakpoint) at  $e_1$ . To make four scrolls, it requires

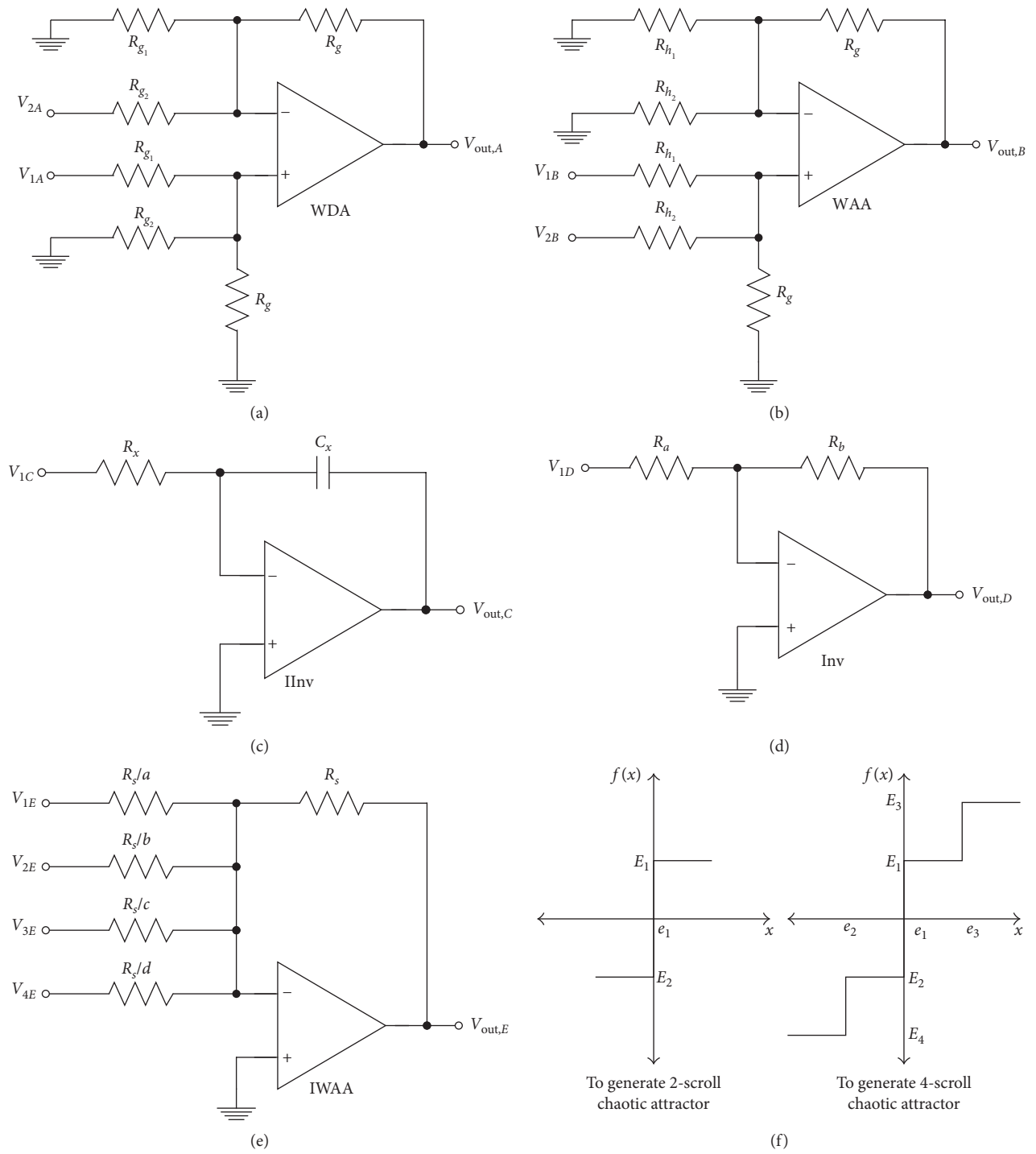


FIGURE 2: Continued.

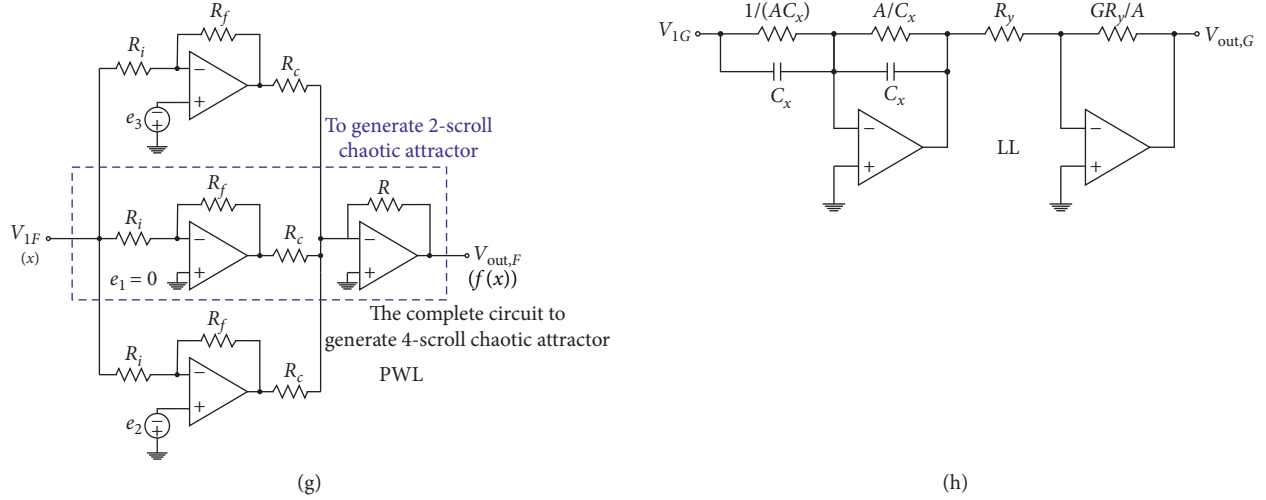


FIGURE 2: Basic building blocks. (a) Weighted differential amplifier (WDA). (b) Two-input weighted adder amplifier (WAA). (c) Inverting integrator (IInv). (d) Inverting amplifier (Inv). (e) Four-input inverting weighted adder amplifier (IWAA). (f) SNLFF for generating two and four scrolls. (g) Circuit realization of SNLFF to generate two and four scrolls. (h) Lead/lag phase network.

four op-amps with four saturated levels at  $E_1, E_2, E_3,$  and  $E_4$  and three shifted voltages at  $e_1, e_2,$  and  $e_3$ .

2.2.7. *Lead/Lag Phase Network (LL)*. The circuit of Figure 2(h) is a particular case of a lead/lag phase network with transfer function

$$\frac{V_{out,G}}{V_{1G}} = G \left( \frac{s+A}{As+1} \right), \quad (12)$$

$$A = \frac{1+\alpha}{1-\alpha},$$

where we can use (8) to translate the frequencies of the zero  $\omega_z = A$  and the pole  $\omega_p = (1/A)$  by a factor  $\Omega$ . It is important to remark that the circuit of Figure 2(h) is an op-amp-based lead compensator, and for the element values as they are labeled in the network, the transfer function becomes (12), which is a scaled version of the approximation in (1).

### 3. Fractional-Order Integrators

This section presents two realizations of fractional integrators using the blocks of Figure 2. We will carry out Monte Carlo and sensitivity analyses in them to study how the uncertainty in the output voltage is allocated to the tolerances of the circuit elements. In addition, we will tune some circuit elements to diminish the slope error in the magnitude frequency response caused by the first-order CFE approximation.

3.1. *Circuit Implementation*. In order to achieve a circuit implementation of the first-order CFE approximation of the fractional integrator given by (1), consider a transfer function in frequency-domain,  $(V_o(s)/V_i(s))$ , expressed in the same form, i.e.,

$$F(s) = \frac{V_o(s)}{V_i(s)} = \frac{s+A}{As+1}, \quad (13)$$

where  $V_i(s)$  and  $V_o(s)$  are input and output voltages. An algebraic manipulation on (13) leads to

$$V_o(s)(As+1) = V_i(s)(s+A), \quad (14)$$

$$sAV_o(s) = sV_i(s) + AV_i(s) - V_o(s),$$

and dividing both sides of (14) by  $As$  and collecting similar terms, we get

$$V_o(s) = \underbrace{\frac{V_i(s)}{A} + \left( \frac{-1}{s} \right)}_{\text{IInv block}} \underbrace{\left[ \frac{V_o(s)}{A} - V_i(s) \right]}_{\text{WDA block}}. \quad (15)$$

WAA block

Figures 3(a) and 3(b) illustrate the corresponding block diagram and electronic realization using circuits WDA, IInv, and WAA. A comparison of (15) with (5) and (6) results in

$$R_{g_1} = R_{h_2} = AR_g, \quad (16)$$

$$R_{g_2} = R_{h_1} = R_g.$$

To determine  $C$  and  $R_x$ , we apply (7) and (8) after designating the degrees of freedom  $C_x$  and  $\Omega$ . Later, once chosen the degree of freedom  $R_g$ , for the order  $\alpha$  required and using (1), we calculate  $R_{g_1} = R_{h_2} = AR_g$  (circuit elements are denoted in blue in Figure 3(b)). The rest of resistances have a value of  $R_g$ . As an example, after adopting the degrees of freedom  $R_g = 100\Omega$ ,  $C_x = 0.1 \text{ mF}$ , and  $\Omega = 1 E_5$ , the resistances  $R_{g_1} = R_{h_2}$  shown in the table of Figure 3(b) result for each order  $\alpha = (0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.85, 0.9, 0.95)$ .

Other alternative of implementation is with the circuit of Figure 2(h) which corresponds to the transfer function (12). To determine  $C$ , we apply (8) after designating the degrees of freedom  $C_x$  and  $\Omega$ . Later, once chosen the degrees of

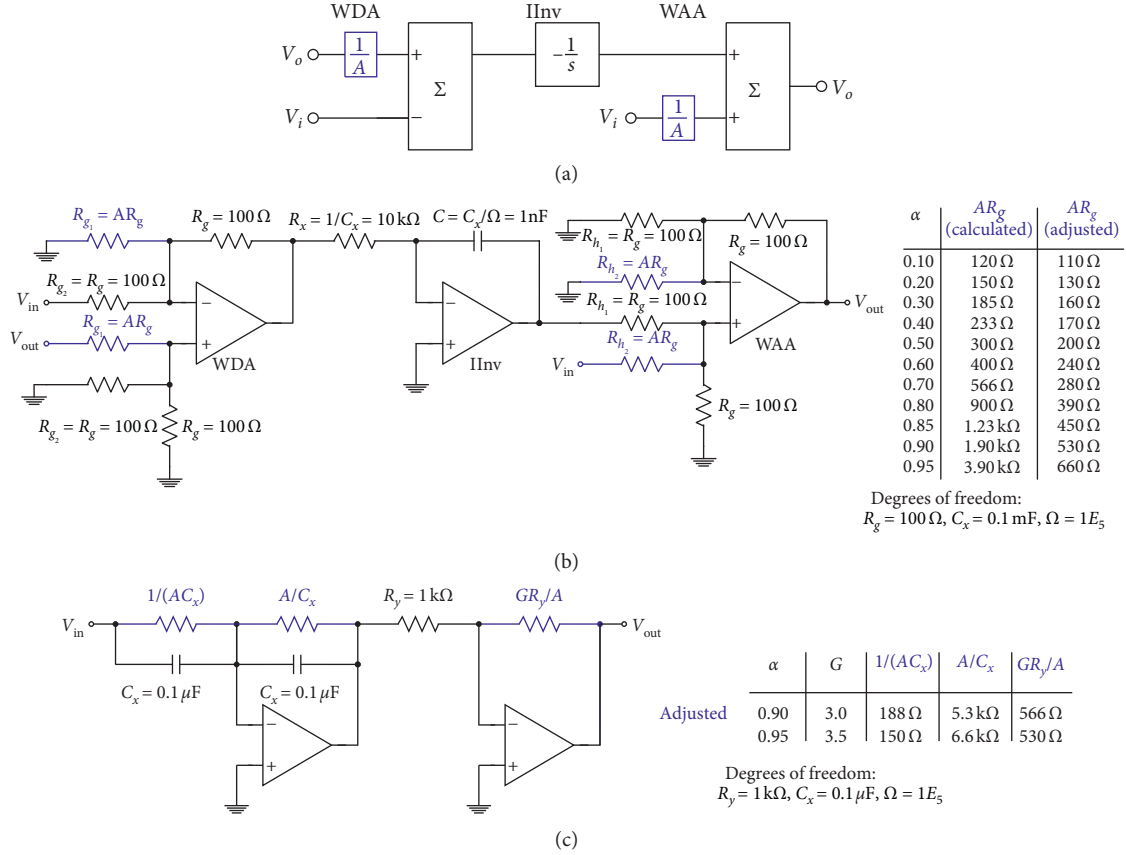


FIGURE 3: Fractional-order integrator. (a) Block diagram. (b) First implementation. (c) Second implementation.

freedom  $R_y$  and  $G$ , for the order  $\alpha$  required and under  $A = ((1 + \alpha)/(1 - \alpha))$ , we calculate  $(1/(AC_x))$ ,  $(A/C_x)$ , and  $(GR_y/A)$  (circuit elements are denoted in blue in Figure 3(c)).

**3.2. Experimental Validation and Slope Adjustment.** We simulated the fractional integrator of Figure 3(b) in HSPICE and breadboarded it with op-amps TL081 (gain bandwidth product = 100 kHz, dc gain = 200 V/V, and supply voltage =  $\pm 15$  V). The input was a sinusoidal voltage with 0.1 V in amplitude and frequency ranged from 1 kHz to 100 kHz. An NI ELVIS II+ laboratory platform provided this signal and bias potentials of  $\pm 15$  V for the op-amps. Figure 4(a) shows the measured frequency responses for  $\alpha = (0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.85, 0.9, 0.95)$ . These plots presented a satisfactory agreement with the results in HSPICE and with numerical simulations of (1) in Matlab. In consequence, the first-order CFE approximation of the fractional integrator causes the slope errors of the frequency responses reported in Table 1, with negligible influence of the circuit elements and no idealities of the op-amps. In agreement with Table 1, these errors are considerable (except for  $\alpha = 0.1$ ,  $\alpha = 0.9$ , and

$\alpha = 0.95$ ), extending from 0.09 dB to 4.73 dB. This performance is prohibitive to carry out chaotic oscillators, which are susceptible to their parameters and initial conditions. To reduce these errors, for each value of  $\alpha$ , we did an experimental tuning of  $R_{g1} = R_{h2} = AR_g$  (see the table of Figure 3(b)). This is equivalent to adjusting  $\alpha$  through  $A$ , getting the frequency responses of Figure 4(b). From this figure and according to Table 1, the adjustment reduces the slope errors to values in the range from  $-0.09$  dB to 0.6 dB, which produces values of  $\alpha$  closer to the theoretical ones. The corresponding curve fitting of Figure 5 brings us a design equation to calculate  $A$  respect to  $\alpha$ , resulting in

$$A(\alpha) = 1.014e^{1.241\alpha} + 0.002697e^{7.48\alpha}, \quad (17)$$

$$\frac{1}{s^\alpha} \approx \frac{s + 1.014e^{1.241\alpha} + 0.002697e^{7.48\alpha}}{(1.014e^{1.241\alpha} + 0.002697e^{7.48\alpha})s + 1}. \quad (18)$$

For the circuit of Figure 3(c) and using the adjusted values of  $A$  of Table 1, for  $R_y = 1\text{k}\Omega$ ,  $C_x = 0.1\mu\text{F}$ , and  $\Omega = 1E_5$ , the resistances of values  $(1/(AC_x))$ ,  $(A/C_x)$ , and  $(GR_y/A)$  shown in the table of Figure 3(c) are obtained. Here,  $\alpha = (0.9, 0.95)$  and  $G = (3, 3.5)$ . Although there are



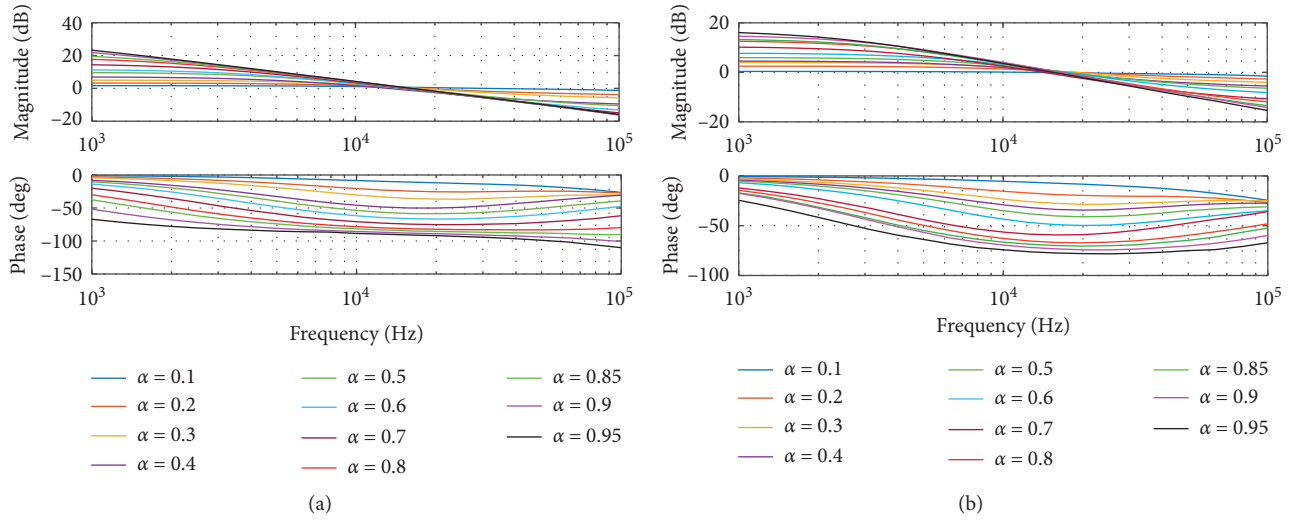


FIGURE 4: Experimental results of the fractional-order integrator: (a) without adjustment and (b) with adjustment.

TABLE 1: A adjustment for each order  $\alpha = (0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.85, 0.9, 0.95)$ .

$\alpha$	Theoretical value		Experimental data without adjustment				Experimental data with adjustment				
	Slope (dB/dec)	$A$	$AR_g$ (k $\Omega$ )	Slope (dB/dec)	Error (dB)	$A$	$AR_g$ (k $\Omega$ )	Slope (dB/dec)	Error (dB)	Phase error (%)	Equivalent $\alpha$
0.10	2	1.20	0.120	2.960	0.96	1.1	0.11	2.140	0.14	-1.12	0.1070
0.20	4	1.50	0.150	6.300	2.30	1.3	0.13	4.170	0.17	-2.57	0.2085
0.30	6	1.85	0.185	8.900	2.90	1.6	0.16	6.600	0.60	-3.16	0.3300
0.40	8	2.33	0.233	11.84	3.84	1.7	0.17	7.910	-0.09	-2.79	0.3955
0.50	10	3.00	0.300	14.53	4.53	2.0	0.20	10.14	0.14	-2.48	0.5070
0.60	12	4.00	0.400	16.73	4.73	2.4	0.24	12.40	0.40	-2.95	0.6200
0.70	14	5.66	0.566	18.38	4.38	2.8	0.28	13.94	-0.06	-2.54	0.6970
0.80	16	9.00	0.900	20.00	4.00	3.9	0.39	16.46	0.46	-2.27	0.8230
0.85	17	12.3	1.230	20.24	3.24	4.5	0.45	17.01	0.01	-3.32	0.8505
0.90	18	19.0	1.900	19.15	1.15	5.3	0.53	18.10	0.10	-0.57	0.9050
0.95	19	39.0	3.900	19.09	0.09	6.6	0.66	19.02	0.02	-0.07	0.9510

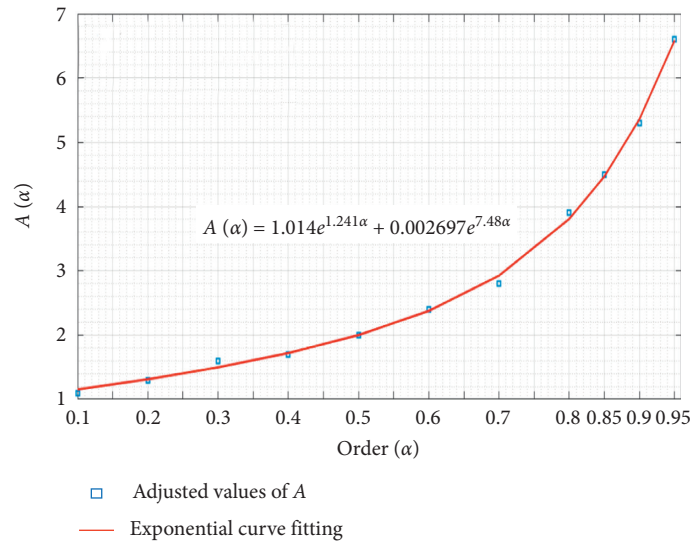


FIGURE 5: Approximation of  $A$  as an exponential function of  $\alpha$ .

other alternatives for implementing fractional-order integrators, as discussed in Section 1, the first-order CFE implementation used in this work is very compact and does not require circuit elements with noncommercial values. Therefore, to the best of the authors' knowledge, this is the first experimental validation of a multiscroll chaotic system based on active fractional-order circuits, and thus, there are not any other works where either simulated or experimental results are reported, and consequently, those cannot be compared with our proposal. In fact, other fractional-order multiscroll chaotic systems based on passive ladder networks as reported in [43, 44] require more hardware, including resistors and capacitors with noncommercial values.

**3.3. Monte Carlo Analysis.** To verify that the circuit of Figure 3(b) is robust to tolerances, we carried out a Monte Carlo analysis in SPICE. We dealt with tolerances of  $\pm 5\%$  and  $\pm 20\%$  in the resistors and capacitors using a normal distribution with  $N=100$ . The variable to examine is the slope of the magnitude response for each value  $\alpha = (0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.85, 0.9, 0.95)$ . To simplify, Figure 6 depicts only the histograms corresponding to the adjusted circuit with  $\alpha = 0.9$  and  $\alpha = 0.95$ . We observe distributions similar to a normal distribution. Table 2 outlines the obtained results for each value of  $\alpha$  and for both cases, with and without adjustment. The resulting standard deviations are small, in the range from 0.027 dB/dec to 0.23 dB/dec, and comparable in both cases. Figure 7(a) illustrates the mean slope obtained for each order. Without tuning, these values move away from the line that describes the theoretical slopes. Figure 7(b) depicts the largest and smallest values that the slope gets without tuning. The maximum error is in the range from 0.5 dB to 4.5 dB. No one order (except  $\alpha = 0.1$ ) encloses the curve of the ideal slope. From Figure 7(c), we observe that the greatest and smallest values of the slope with tuning are closer to the ideal line, enclosing it. The maximum error is in the range of 0.6 dB. This way, the error in the first-order CFE approximation without adjustment influences the slope more than the tolerances.

**3.4. Sensitivity Analysis.** In assessing the sensitivity of the output voltage of the fractional-order integrator of Figure 8 regarding its resistive elements, by performing a normalized sensitivity simulation, the results reported in Table 3 are achieved. Note that only four of the thirteen resistors of the circuit are in Table 3 since these are those who exhibit a "major" impact on the integrator's sensitivity. As appreciated, different scenarios may occur depending on the value of  $\alpha$ , but in general terms sensitivity is a little less when the adjustment has been applied. Without loss of generality, we can say that the larger the value of  $\alpha$  is, the larger the sensitivity becomes. Still, sensitivity is highly acceptable. Let us take the worst case when  $\alpha = 0.95$  and a 1% variation of the nominal value of  $R_{G_{02}}$  produces a deviation of  $\approx 2.3$  mV in the output voltage of the circuit. Even though this value is low, a lesser variation can be attained if a high-precision resistor (with a tolerance  $< 1\%$ ) is used for  $R_{G_{02}}$ . We can apply

the same criteria for the rest of the resistors in terms of tolerances; however, there is a trade-off between sensitivity and realization cost, and high-precision resistors are also more expensive. It is important to emphasize that the sensitivity of the output voltage at a frequency of 0 Hz ( $\omega = 0$  rad/s), i.e., at DC regime, and  $V_{in} = 1$  V is equivalent to determine the sensitivity of the transfer function,  $F(s)$ , when  $s = j\omega = 0$ , i.e., for  $F(0) = A$ . And thus, we are evaluating  $A$  variation as a function of the resistive elements.

To evaluate the sensitivity of the fractional-order integrator regarding capacitor  $C_x$ , Figure 9 depicts the behavior of the normalized sensitivity of  $F(s)$  for both with and without adjustment of parameter  $A$ . We define the normalized sensitivity as

$$S_{C_x}^{F(s)} = \frac{C_x}{F(s)} \frac{dF(s)}{dC_x}, \quad (19)$$

with nominal values  $C_x = 1$  nF and  $s = 2\pi(15.91 \text{ kHz})j$ , and with  $F(s)$  given by (13). As illustrated, the tendency is rising towards the 1% of  $F(s)$  variation as  $C_x$  changes 1% of its nominal value along with the  $\alpha$  increment.

According to the results reported above, we can conclude that the proposed fractional-order integrator exhibits a low sensitivity regarding variations of the values of its passive elements.

## 4. Fractional-Order Multiscroll Lü Chaotic System

In this section, we design electronic circuits based on the building blocks of Figure 2 and the fractional integrators of Figure 3 to realize commensurate fractional-order Lü chaotic system, i.e., system with equal fractional order for integrators. A commensurate realization is acceptable to test the functionality and benefits of using the active fractional-order integrators of Figure 3, but incommensurate fractional-order oscillators, as those reported in [45–47] or [48] can also be realized with the proposed approach without increasing hardware requirements. In fact, the proposed approach is an attractive alternative for the design of incommensurate fractional-order oscillators because it is necessary to calculate the parameter  $A$  using (17) instead of designing ladder networks.

The fractional-order Lü chaotic system is a realization that represents the transition from the Lorenz to the Chen attractor [49, 50]. The Lü system displays the following system of equations:

$$\begin{aligned} D^\alpha x &= y, \\ D^\alpha y &= z, \\ D^\alpha z &= -ax - by - cz + d_1 \frac{f(x)}{\text{PWL}}, \end{aligned} \quad (20)$$

where  $x$ ,  $y$ , and  $z$  are state variables,  $a$ ,  $b$ ,  $c$ , and  $d$  are positive real constants,  $\alpha \in (0, 1)$  is the fractional order, and  $f(x)$  is a SNLF similar to that represented in Figure 2(f). In [43, 49], the authors determine, for a Lü chaotic oscillator, the suitable incommensurate fractional order to preserve the



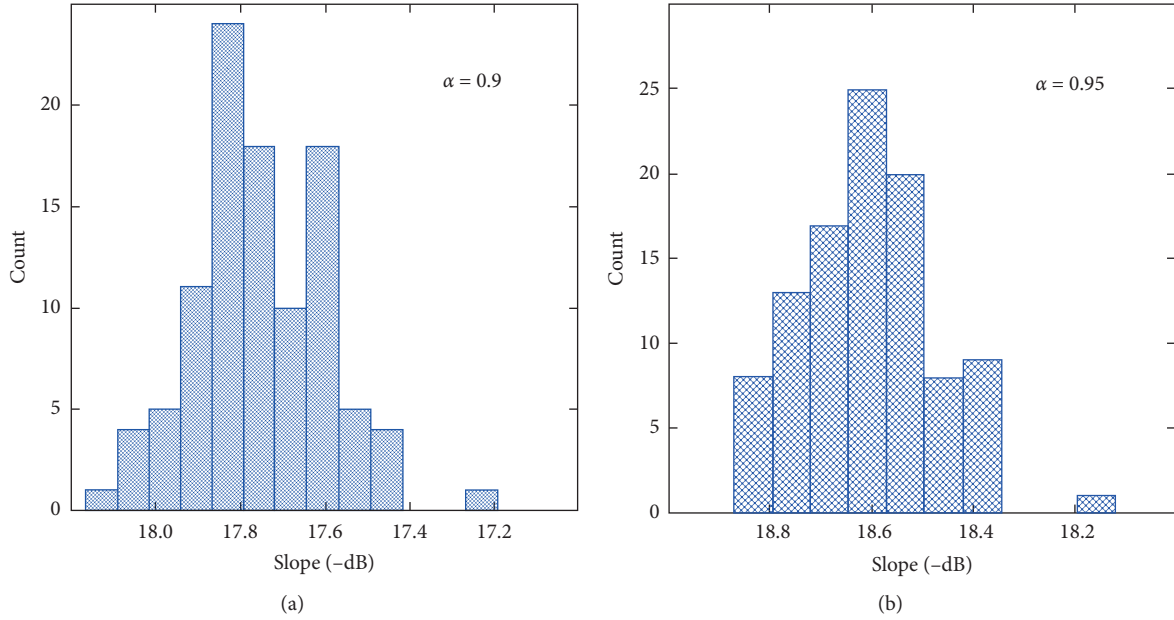
FIGURE 6: Histograms (Monte Carlo analysis): (a)  $\alpha = 0.9$  and (b)  $\alpha = 0.95$ .

TABLE 2: Monte Carlo analysis.

$\alpha$	Without adjustment				With adjustment			
	Mean slope (dB/dec)	Std. dev. (dB/dec)	Min. (dB/dec)	Max. (dB/dec)	Mean slope (dB/dec)	Std. dev. (dB/dec) (m)	Min. (dB/dec)	Max. (dB/dec)
0.10	-2.54	200.62	-3.04	-1.94	-1.90	189.72	-2.35	-1.41
0.20	-5.77	177.18	-6.12	-5.30	-3.77	197.33	-4.24	-3.33
0.30	-8.65	204.31	-9.18	-8.23	-6.73	177.47	-7.13	-6.24
0.40	-11.45	167.15	-11.92	-11.03	-7.57	175.89	-7.95	-7.09
0.50	-14.00	213.91	-14.55	-13.53	-9.65	187.33	-10.10	-9.11
0.60	-16.29	153.06	-16.56	-15.86	-11.8	159.39	-12.28	-11.43
0.70	-18.13	90.907	-18.28	-17.76	-13.39	151.61	-13.74	-13.00
0.80	-19.17	167.37	-19.54	-18.64	-15.91	238.89	-16.49	v15.30
0.85	-18.50	167.71	-18.92	-18.08	-16.89	180.43	-17.16	-16.44
0.90	-19.30	97.381	-19.50	-18.97	-17.75	153.82	-18.00	-17.26
0.95	-19.83	27.705	-19.89	-19.73	-18.60	129.53	-18.85	-18.17

chaotic behavior with  $(a, b, c, d) = (2, 1, 0.6, 2)$ , getting  $\alpha_1 = 0.8$ ,  $\alpha_2 = 0.9$ , and  $\alpha_3 = 0.95$  and Lyapunov exponents  $LE_1 = 0.3226$ ,  $LE_2 = 0$ , and  $LE_3 = -1.2203$ . Taking as reference that design, we will design our 2-scroll and 4-scroll commensurate realizations with the same parameters  $a$ ,  $b$ ,  $c$ , and  $d$ , and with  $\alpha = 0.9$  and  $\alpha = 0.95$ . The stability can be verified by using the method reported in [51].

Figure 10 depicts the block diagram and design details of the commensurate fractional-order system in (20). Figure 11 shows the corresponding experimental setup with fractional integrators as those depicted in Figure 3(b) and all the circuits realized using TL081 op-amps. The setup comprises a Keysight DSOX3054A oscilloscope, two DC power supplies RIGOL DP832 and BK precision 1550, and the PCB realized with the software Altium Designer 19. The design details of the PWL block for a 4-scroll chaotic attractor are presented in this figure for a saturation voltage  $V_{\text{sat}} = 13.5V$ .  $V_{\text{CC}}$  and  $V_{\text{EE}}$  are the bias voltages of the op-amps TL081, while  $V_+$  and  $V_-$  are the voltages required by the block  $f(x)$ .

The 2-scroll chaotic attractor can be obtained with this circuit, as is illustrated in Figure 2(g). The four-input IWAA is designed with the degree of freedom  $R_g = 1 \text{ k}\Omega$  and the desired values for  $a$ ,  $b$ ,  $c$ , and  $d$ . We incorporated a gain  $G$  to the first and second approximations of the fractional integrator to add tuning capacity. The parameter  $A$  was calculated using (17) and the degrees of freedom for the first approximation were  $R_g = 100 \Omega$ ,  $C_x = 0.1 \text{ mF}$ ,  $\Omega = 1 E_5$ ,  $C = 1 \text{ nF}$ , and  $R_x = 5 \text{ k}\Omega$ . For the second approximation, we used  $R_y = 1 \text{ k}\Omega$ ,  $C_x = 0.1 \mu\text{F}$ ,  $\Omega = 1 E_5$ , and  $C = 1 \text{ pF}$ . Values of  $G = 3$  and  $G = 3.5$  were used for  $\alpha = 0.9$  and  $\alpha = 0.95$  to approximate the frequency response of the integrators to the response of equivalent passive realizations. We can observe that, with the first approximation, the chaotic oscillator requires for implementation 54 resistors, 3 capacitors, and 14 op-amps. With the second approximation, the circuit comprises 27 resistors, 6 capacitors, and 11 op-amps. Figures 12(a) and 12(b) show the SPICE simulation and experimental measurement of the 2-scroll chaotic attractor

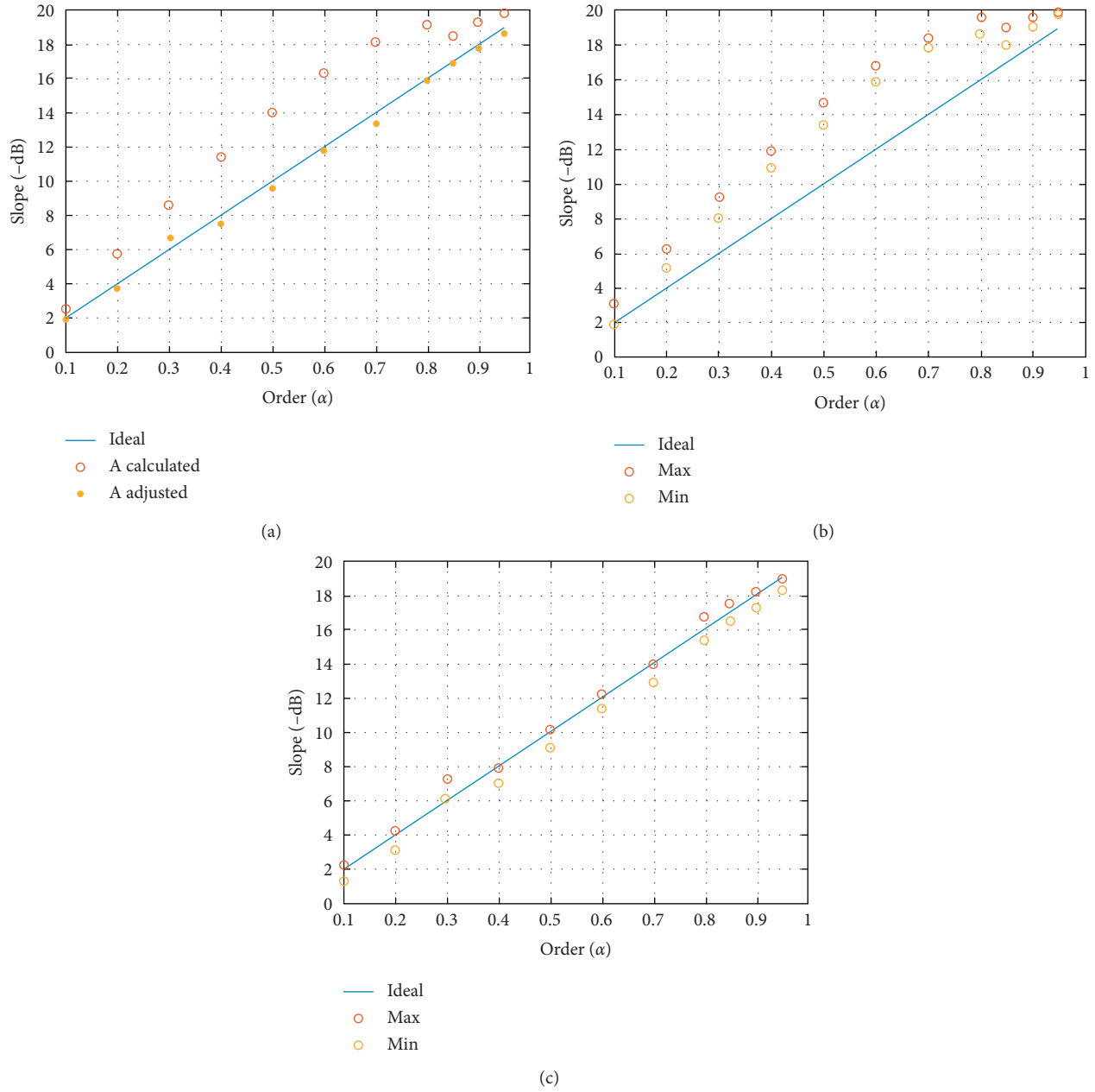


FIGURE 7: Monte Carlo analysis: (a) mean values of slope with and without adjustment. (b) Maximum and minimum values of slope without adjustment. (c) Maximum and minimum values of slope with adjustment.

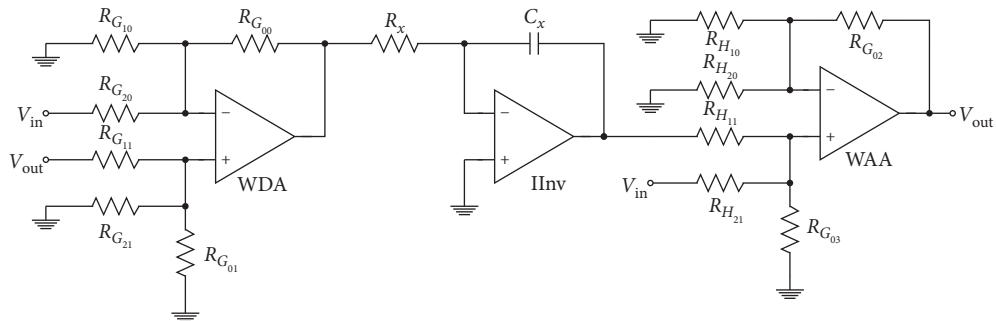


FIGURE 8: Fractional-order integrator: notation for the sensitivity analysis.

TABLE 3: Sensitivity analysis.

Order $\alpha$	Sensitivity without adjustment				Sensitivity with adjustment			
	$R_{G_{02}}$ (mV/%)	$R_{G_{11}}$ (mV/%)	$R_{G_{20}}$ (mV/%)	$R_{H_{10}}$ (mV/%)	$R_{G_{02}}$ (mV/%)	$R_{G_{11}}$ (mV/%)	$R_{G_{20}}$ (mV/%)	$R_{H_{10}}$ (mV/%)
0.10	—	8.47	-7.77	—	—	7.56	-7.22	—
0.20	—	11.3	-9.38	—	—	9.39	-8.31	—
0.30	—	14.6	-11.2	—	—	12.2	-9.91	—
0.40	—	19.2	-13.7	—	—	13.1	-10.4	—
0.50	11.4	8.56	$2.6e-13$	6.42	$2.95e-4$	16.0	-12.0	$-1.96e-4$
0.60	13.1	8.38	$-7.75e-5$	8.37	$4.08e-4$	19.9	-14.1	$-2.88e-4$
0.70	15.2	7.74	$-1.28e-4$	10.9	$5.4e-4$	23.8	-16.1	$-3.98e-4$
0.80	17.8	6.40	—	14.3	13.0	8.41	—	8.19
0.85	19.4	5.37	—	16.4	13.8	8.21	—	9.22
0.90	21.2	4.00	—	18.8	14.8	7.89	—	10.4
0.95	23.3	22.3	—	21.4	16.1	7.34	—	12.1

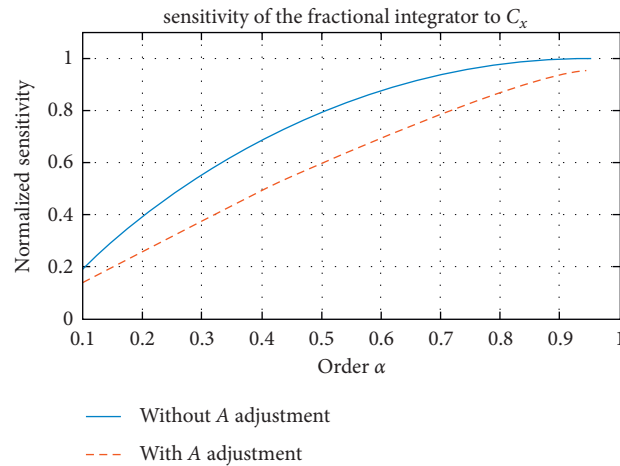


FIGURE 9: Normalized sensitivity of  $F(s)$  regarding  $C_x$ .

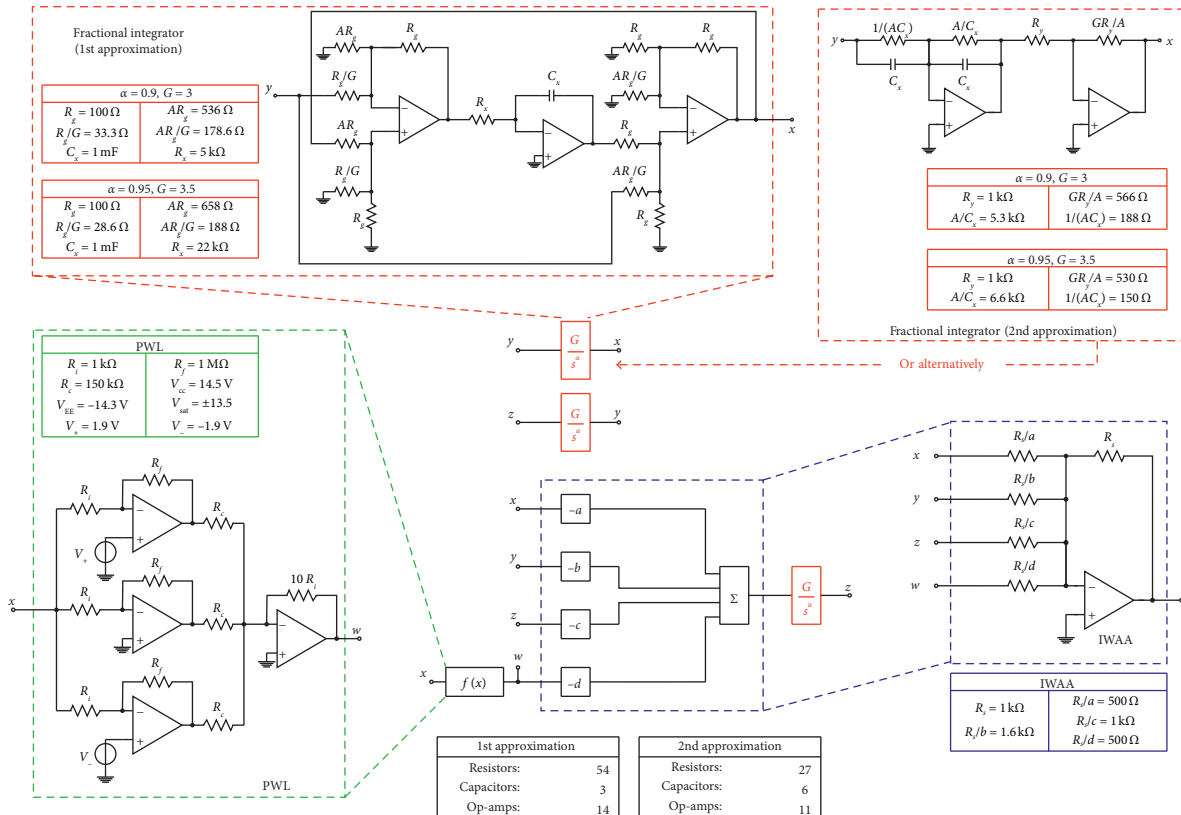


FIGURE 10: Block diagram and circuit synthesis to realize the fractional-order multiscroll PWL Lü chaotic system in (20) with  $\alpha = 0.9$  and  $\alpha = 0.95$ .

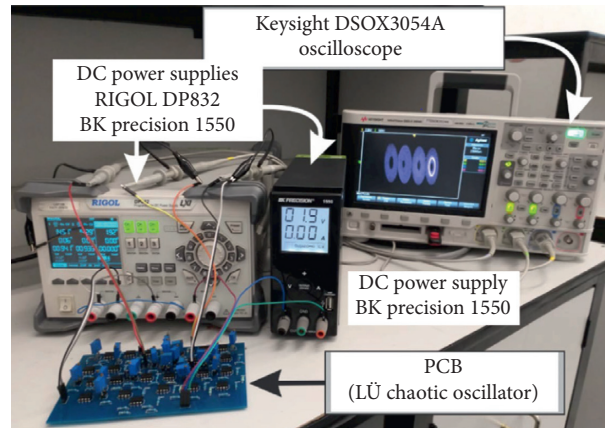


FIGURE 11: Experimental setup.

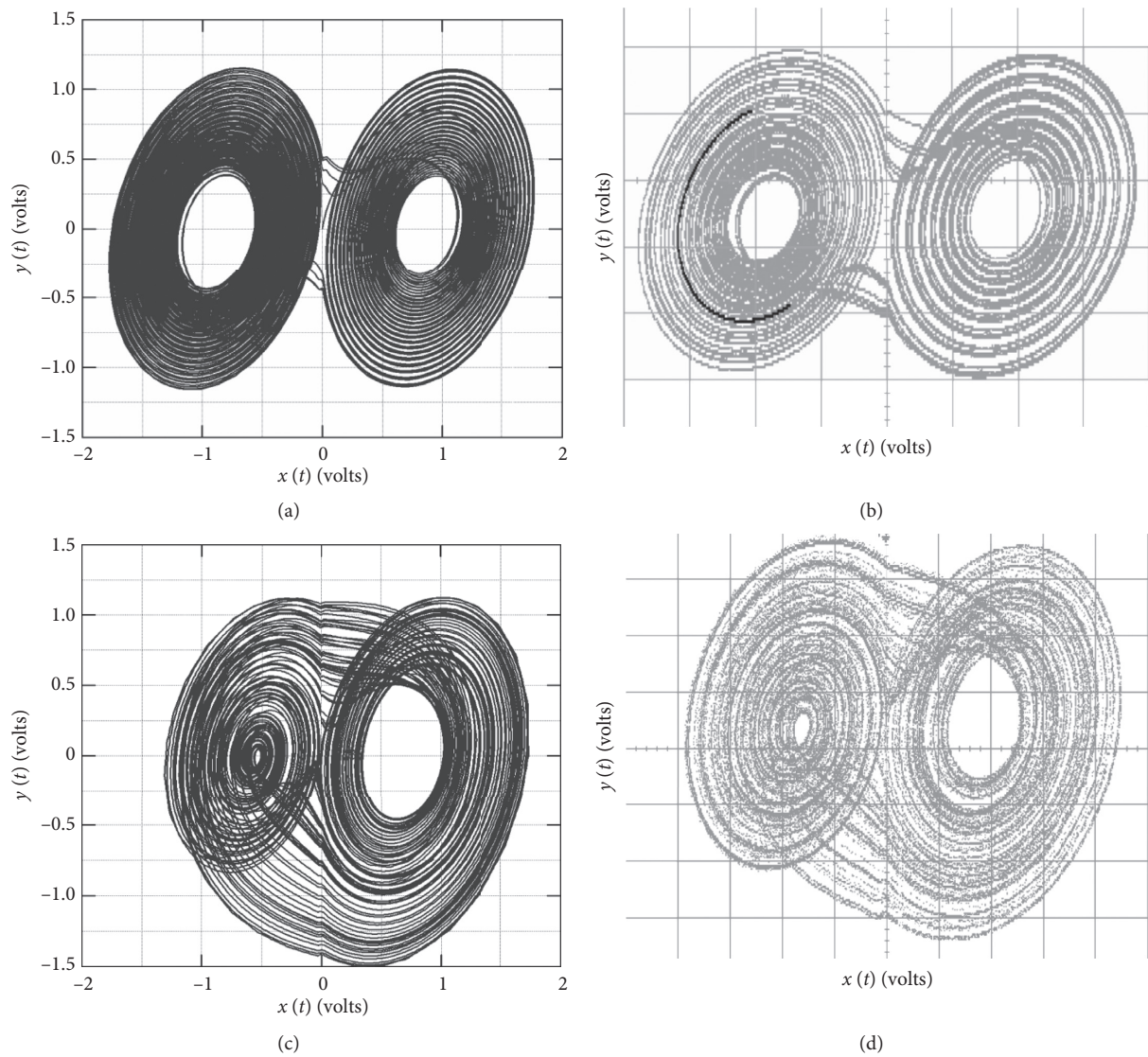


FIGURE 12: Projection of the 2-scroll chaotic attractor onto  $xy$ -plane (phase space portrait): (a) simulation result with  $\alpha = 0.9$  (SPICE); (b) experimental result with  $\alpha = 0.9$  (oscilloscope scale = 0.5 V per division); (c) simulation result with  $\alpha = 0.95$  (SPICE); (d) experimental result with  $\alpha = 0.95$  (oscilloscope scale = 0.3 V per division).



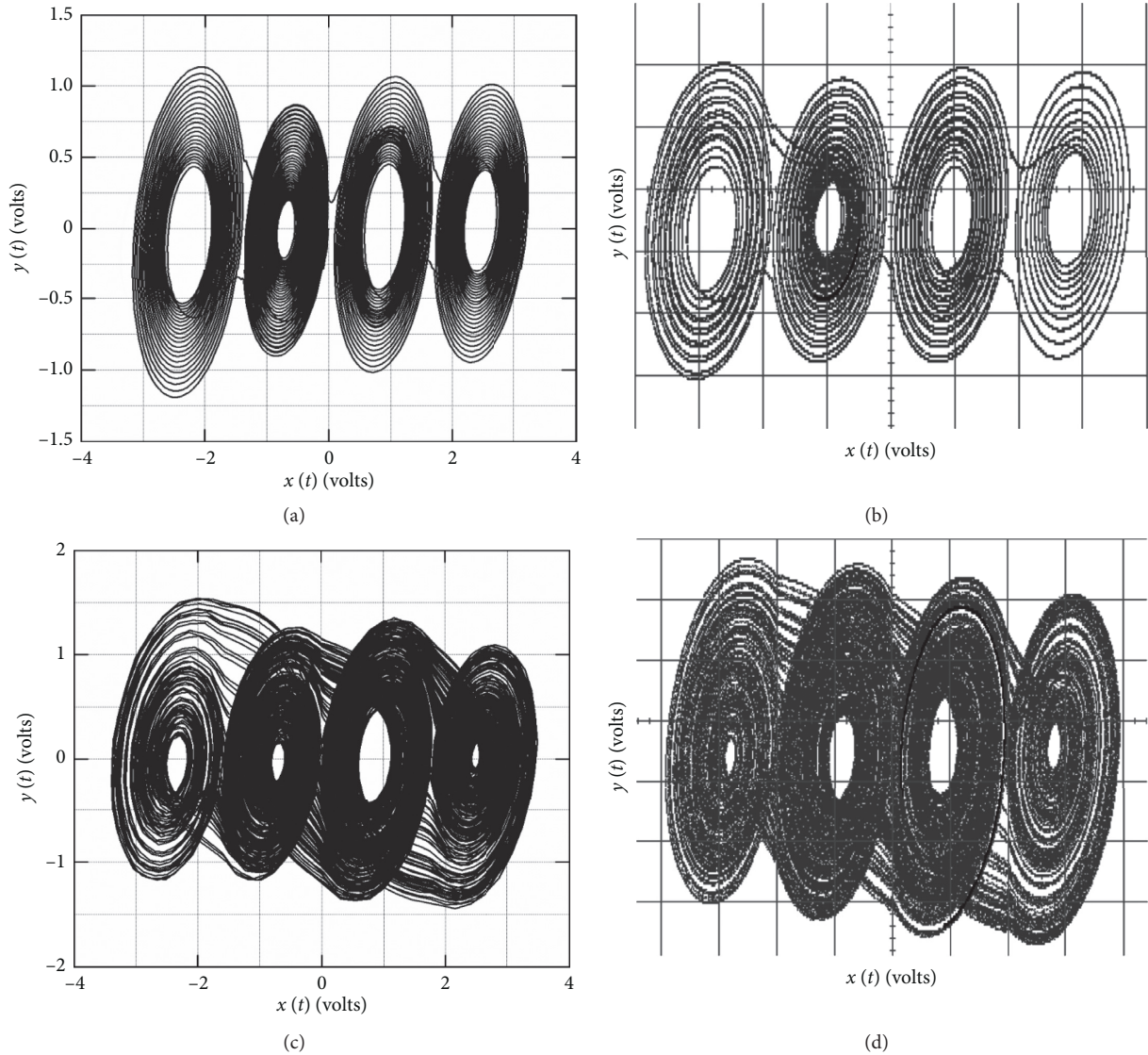


FIGURE 13: Projection of the 4-scroll chaotic attractor onto  $xy$ -plane (phase space portrait): (a) simulation result with  $\alpha = 0.9$  (SPICE); (b) experimental result with  $\alpha = 0.9$  (oscilloscope scale = 1 V per division); (c) simulation result with  $\alpha = 0.95$  (SPICE); (d) experimental result with  $\alpha = 0.95$  (oscilloscope scale = 1 V per division).

TABLE 4: Comparison of hardware requirements of implemented Lü fractional-order chaotic oscillators.

Realization	Number of resistors			Number of capacitors			Op-amps
	Commercial	Noncommercial	Total	Commercial	Noncommercial	Total	
[43]	33	11	44	0	11	11	15
[44]	16	17	33	0	9	9	15
1st approximation	42	12	54	3	0	3	14
2nd approximation	18	9	27	6	0	6	11

projected onto  $xy$ -plane (phase space portrait) for  $\alpha = 0.9$ . Figures 12(c) and 12(d) show the SPICE simulation and experimental measurement of the same projection for  $\alpha = 0.95$ . We can observe an agreement between simulation,

theoretical, and experimental results. Figures 13(a) and 13(b) show the SPICE simulation and experimental measurement of the projection of the 4-scroll chaotic attractor onto  $xy$ -plane for  $\alpha = 0.9$ . Figures 13(c) and 13(d) show the



SPICE simulation and experimental measurement of the same projection for  $\alpha = 0.95$ . Again we observe agreement between simulation and experimental results.

Table 4 shows a comparison of the hardware requirements of the two proposed realization and the fractional-order oscillators reported in [43, 44]. Despite the active realization of the fractional integrators, we observe that the two proposed implementations reduce the number of required op-amps (reducing power consumption), do not require noncommercial capacitors, and have a comparable number of noncommercial resistors. Unlike the resistors used in [43, 44], the values of the noncommercial resistors of the proposed realizations are easy to approximate with combinations of commercially available resistors, avoiding bulky realizations difficult to redesign. Another advantage is the easy design of the fractional-order integrators using (17) instead of calculating the elements of ladder networks.

## 5. Conclusion

This paper presented the design and electronic implementation of a commensurate fractional-order multiscroll chaotic oscillator with orders  $\alpha = 0.9$  and  $\alpha = 0.95$ . The fractional-order integrators realized with tuned first-order active realizations are robust to tolerances in the passive elements and favor the use of resistors and capacitors with commercial values, reducing hardware requirements and design and implementation efforts. The easy design of the fractional-order integrators with improved accuracy using (17) instead of calculating ladder networks could favor the practical realization of other types of systems, such as incommensurate chaotic oscillators, fractional-order filters, fractional-order controllers, and fractional-order memristors.

Finally, the physical realization of fractional-order chaotic systems with hidden dynamics (attractors without equilibrium points, multistability, extreme multistability, etc.) along with their synchronization schemes using the proposed approach will be conducted in future works to explore secure communications based on fractional chaos.

## Data Availability

The necessary data are included within the article.

## Conflicts of Interest

The authors declare no conflicts of interest.

## Acknowledgments

This work was supported by projects CONACYT (258880), Plan de Trabajo CA (BUAP-CA-276) by SEP-PRODEP, and VIEP-BUAP.

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