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Robust single-phase inverter based on the buck–boost converter through an efficient hybrid control

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Abstract: This study presents a new and robust single-phase inverter based on the buck–boost converter. The proposed inverter topology has minimised numbers of active and passive elements that provide less complexity and cost. Unlike similar studies in the literature, an efficient hybrid control technique is used for the control of the inverter operation. The hybrid control technique is comprised of the traditional feedback proportional–integral–derivative (PID) controller and the new proposed open-loop control technique called 'control law'. This hybrid control technique provides stable and high response performance operation for the proposed inverter while the system parameters change. The proposed inverter can operate with a wide range of output frequency and output voltage value on different load conditions while satisfying <5% voltage total harmonic distortion (THD) value of the output voltage. An experimental laboratory setup with the values of 0.5 kW, 0–100 V_p and 0–50 Hz is built for the proposed inverter. The experimental results demonstrate that the proposed inverter can produce high-quality output voltage with <5% THD on different input and output system parameters.

1 Introduction

As the inverters have a wide application area, there are many increasing inverter studies in the literature. The fundamental target of these studies is producing an alternative voltage as far as possible close to sine form with low total harmonic distortion (THD) value on different system conditions at the output of the inverter, also developing the inverter topology with fewer elements and complexity. For this aim, many inverter topologies and operation techniques are developed. However, each study to improve the output voltage quality causes increasing elements number and complexity or vice versa. So, these targets must be considered together and determining the optimal solution is the best way according to the demands.

Pulse-width modulation (PWM) technique-based inverters are the well known and most applied ones in practise [1]. In PWM inverters, the output voltage is alternative that is comprised of modulated square-wave produced from the direct input voltage. So the produced inverter output voltage is far from sine wave with high THD value in these inverters. Many PWM techniques are developed to reduce the voltage THD values such as sine–triangle comparison [2] and selective harmonic elimination method [3]. However, even so, the inverter output voltage is still far from sine wave with these techniques. So, in many applications, the designers have used a coupling transformer close to sine wave [4] but it is clear that this solution increases both the size and the cost of the inverter. Pulse-amplitude modulation (PAM) technique is another one that is applied on inverters to enhance the output voltage quality and is more efficient than PWM technique [5]. In PAM technique, the aim is to produce an inverter output voltage step by step with different direct voltage values close to sine wave. This is provided through either series connected more than one inverters with coupling transformers or cascade-connected capacitor topologies [6, 7]. In both the two ways, the price of closing to sine wave is increasing the number of the direct voltage steps, so is increasing the cost, size and complexity of the inverter. Despite all of the mentioned disadvantages of PWM and PAM inverters, the main advantage of these inverters is that the output voltage can be produced independently of the load and no feedback control is required.

The increasing development and studies on DC–DC converters lead the researchers to modify and operate these converters in inverter mode for a long time. There are many successful studies on such as buck [8–10], boost [11–13] and Ćuk [14–16] converters based inverters in the literature. The switch-mode characteristics with high frequency through the main inductor–capacitor low-pass filter structure of these inverters provide producing very close to sine form with very low THD values without need of coupling transformer or any addition passive filter at the output of these inverters according to the PWM-type and PAM-type inverters. However, because of their specific structure, the output voltage strictly depends on the load. Also, the highly non-linear structure of these inverters makes difficult to control the operation. So, efficient, complex and difficult feedback control is required considering the load and other system parameters change. Generally, it is not possible by only traditional feedback controllers when the system parameters change during operation. Since the traditional controllers are designed for determined system parameters set according to the required response performance. So, when any system parameter changes, the mathematical model of course changes. Thus, the determined controller parameters cannot meet the required response performance or the system may lead to instability.

Many types of buck–boost converter-based single-phase inverters with various topologies are also studied well in the literature. These inverters are superior to the buck-type and boost-type inverters mentioned above on producing a wide amplitude range output voltage as they have both bucking and boosting structures together. Although the Ćuk inverters have the same buck and boost features, it is clear that they have more active and passive elements and this causes more complexity and cost according to the buck–boost inverters. The existing studies on single-phase inverters based on buck–boost converter have superiorities and lacks according to each other.

Lee *et al.* [17] and Qin *et al.* [18] proposed different single-phase buck–boost inverter topologies but same as including four active switches, two diodes, two inductors and two capacitors. Khan and Cha's [19] inverter topology includes four active switches, four diodes, six inductors and three capacitors. Kumar and Sensarma [20] present a topology with four active switches, two inductors and three capacitors. The topology proposed by

Darwish *et al.* [21] includes two active switches, two inductors and two capacitors. Nishad and Shafeeque [22] propose a topology that consists of six active switches, two diodes, one inductor and one capacitor. Todkar and Shinde's [23] inverter uses four active switches, one diode, two inductors and two capacitors. Chang *et al.* [24] propose an inverter topology that includes six active switches, one diode, two inductors and two capacitors. Gandomi *et al.* [25] present a topology with five active switches, one inductor and one capacitor. Atly and Aathira's [26, 27] inverters have eight active switches, one inductor and one capacitor. Tang *et al.* [28] give a different inverter topology including four active switches, one inductor, one capacitor and additionally one coupling transformer. In these studies mentioned here, only the inverter topologies and their operation procedures are given. The elements of the topologies are considered ideal, so, the real parasitic components are ignored in the studies. The dynamic analyses are not done, and the transfer functions of the inverters are not determined. Moreover, the feedback control techniques are not given in these studies.

Sreekanth *et al.* [29] develop a topology with six active switches, four inductors and two capacitors demonstrating the real parasitic components in the topology. However, these parasitic components are not considered in the mathematical calculations. However, the dynamic equations are not given in the calculations. Proportional–integral (PI) controller is applied for the feedback control of the inverter but the detailed controller design analyses are not given. Ho and Siu [30] proposed a topology with six active switches, two inductors and one capacitor and Krishnapriya *et al.* [31] presents an inverter including six active switches, six diodes, one inductor and one capacitor. In these two studies, the real parasitic components are ignored in the topologies. The dynamic equations and the transfer functions are not obtained. The feedback PI controller is used in the studies but the design procedures are not determined.

Ibrahim *et al.* [32] studies on a topology consist of four active switches, two diodes, two inductors and two capacitors. In the study of Sari and Chandrabose [33], four active switches, two inductors and one capacitor are used in the presented topology. The two studies give the detailed dynamic analyses of the proposed inverter topologies but the real parasitic effects are not considered in the calculations. On the other hand, the feedback control of the inverters is not presented.

Xu *et al.* proposed a topology including four active switches, two inductors and two capacitors [34]. In this paper, detailed dynamic analyses are given but the real parasitic effects are ignored. The large-signal analysis is done for determining the inverter transfer function but the small-signal analysis is absent. On the other hand, any information about the feedback control of the inverter does not exist. Sreekanth *et al.* [35] give another inverter that uses five active switches, two diodes, two inductors and one capacitor. This study also gives detailed dynamic analyses but ignoring the real parasitic components. PI controller is used for the feedback control of the inverter but the transfer functions of the inverter and the controller design procedure are not derived in the study. The studies of Husev *et al.* [36, 37] present a topology that includes eight active switches, six diodes, four inductors and four capacitors. The small-signal dynamic analyses and Bode analyses are given in detail but the small-signal transfer functions are not derived. Also, the feedback control structure and control design are not analysed. Another study of Xu *et al.* proposes an inverter including three active switches, one inductor, one capacitor and one coupling transformer [38].The study ignores the parasitic components of the inverter's elements. The dynamic analysis and transfer function analysis are not done. The inverter uses a combined PI controller-based feedback control and energy modulation-based open-loop control technique. However, the detailed control design analysis is not given.

In this paper, a new single-phase inverter topology based on buck–boost converter is proposed. The proposed inverter has the superiorities and the additional advantageous features according to the similar studies detailed reviewed above as follows. The proposed inverter has minimal number of elements consisting of eight active switches, one inductor and one capacitor is proposed. Series Resistor-Inductor-Diode (RLD) and parallel Resistor-Capacitor-Diode (RCD) snubber circuits are designed for each active switch considering the main inverter topology. The snubber circuits provide zero-current and zero-voltage switching for the active switches dissipating the switching loses from the switches to the snubber circuits. Thus, heating problem caused by switching losses is prevented on the switches. On the other hand, the designed parallel RCD snubber circuits protect the switches from overvoltages during off switching. So, safety inverter operation is provided by the snubber circuits. The detailed inverter dynamic equations considering the real parasitic effects of the elements are obtained to be valid in real-time practical applications. The small-signal linearised transfer function of the inverter is derived for the feedback control design. Unlike similar studies in the literature, an efficient hybrid control technique is used for the control of the inverter operation. The hybrid control technique is comprised of the traditional feedback PI derivative (PID) controller and the new proposed open-loop control technique called as 'control law (CL)'. This hybrid control technique provides stable and high response performance operation for the proposed inverter while the system parameters change. Since when the system parameters used in feedback PID controller design change anytime in operation, the mathematical model changes and the determined PID controller cannot meet the required response performance. The proposed open-loop CL technique produces a supporting signal to the PID controller to obtain the required switching duty ratio of new operation point. The proposed inverter can operate with a wide range of output frequency and output voltage value on different load conditions while satisfying <5% voltage THD value of the output voltage. An experimental laboratory setup with the values of 0.5 kW, 0–100 V_p and 0–50 Hz is built for the proposed inverter. The experimental results prove that the proposed inverter can produce high-quality output voltage with <5% THD on different input and output system parameters in a robust and efficient manner.

2 Proposed single-phase inverter

This section describes the topology of the proposed single-phase inverter based on buck–boost converter, the main operation procedure of the inverter and the dynamic analysis of the inverter circuit.

2.1 Proposed topology

The general circuit representation of the proposed inverter is given in Fig. 1 [39]. In Fig. 1, E, $V_i(t)$, $V_s(t)$, $V_o(t)$, L and C represent the direct voltage source, inverter input voltage, input voltage of S_5 switch, inverter output voltage, inductor and the capacitor, respectively. In this paper, direct voltage source of the inverter is considered as battery. In practical, the source may be a time-variant voltage source. As seen from Fig. 1, the inverter input voltage equals to the source voltage

$$V_i(t) = E \tag{1}$$

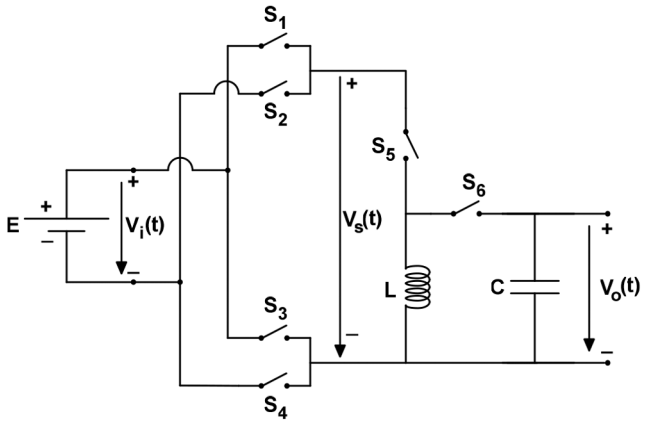

Fig. 1 *General circuit representation of the proposed inverter*

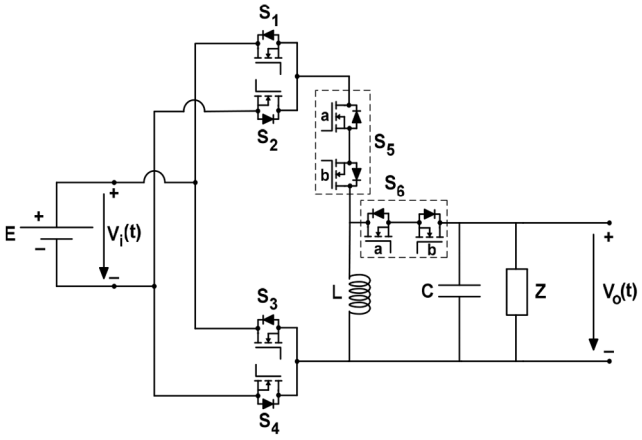

Fig. 2 *Proposed inverter topology using MOSFETs*

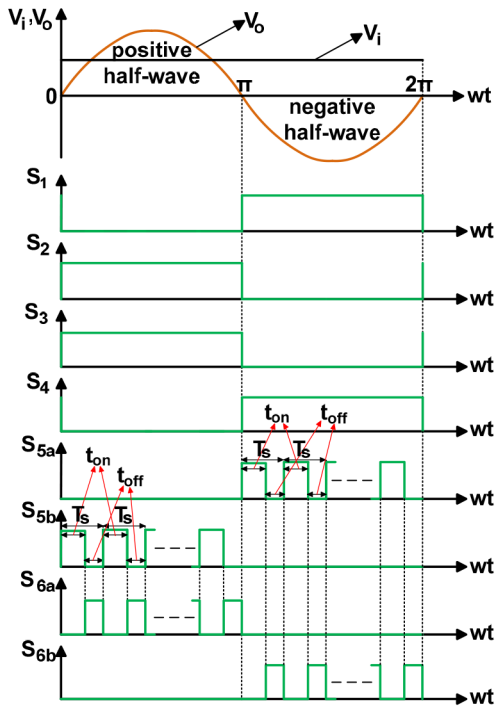

Fig. 3 *Switching pattern of the MOSFETs during inverter operation*

In Fig. 1, S_1, S_2, S_3 and S_4 represent the unidirectional active switches. S_5 and S_6 represent the bidirectional active switches. In the proposed topology, high-speed metal–oxide–semiconductor field-effect transistors (MOSFETs) including antiparallel diodes are used for bidirectional active switches. So, the proposed main inverter topology using MOSFETs is shown in Fig. 2.

In Fig. 2, Z represents the output load, the load may be ohmic, inductive or capacitive. The bidirectional S_5 and S_6 active switches are built by two back-to-back MOSFETs.

2.2 Main inverter operation procedure

The main inverter operation procedure can be explained through the general circuit given in Fig. 1. The inverter operation is based on the well known buck–boost converter through controlling the S_5 switch [40]. When S_5 is turned on and so S_6 is turned off, input voltage supplies the inductor and the inductor is energised. In this case, the output load is supplied through the already pre-charged capacitor. When S_5 is turned off and so S_6 is turned on, the pre-energised inductor supplies both the capacitor and output load. Thus, the input voltage is bucked or boosted at the output of the inverter depending on the duty ratio of S_5 switch.

As the target is producing a sine wave, so an alternative voltage at the output from the direct input voltage, the voltage at the input of S_5 must be alternated. If S_1 and S_4 are turned on, S_2 and S_3 are turned off, the polarity of $V_s(t)$ is positive, the same with the polarity of $V_i(t)$. In this case, the produced output voltage $V_o(t)$ becomes negative according to the determined polarity given in Fig. 1. If S_1 and S_4 are turned off, S_2 and S_3 are turned on, the polarity of $V_s(t)$ is negative, the opposite of the $V_i(t)$ polarity. In this case, the produced output voltage $V_o(t)$ becomes positive according to the determined polarity given in Fig. 1. As seen from Fig. 2, to make S_5 turned on when $V_s(t)$ is positive, S_{5a} is turned on and S_{5b} is turned off. To make S_6 turned on when $V_s(t)$ is positive, S_{6b} is turned on and S_{6a} is turned off. When $V_s(t)$ is negative, S_{5b} is turned on and S_{5a} is turned off to make S_5 turned on. To make S_6 turned on when $V_s(t)$ is negative, S_{6a} is turned on and S_{6b} is turned off. In any case $V_s(t)$ is positive or negative, S_{5a} and S_{5b} are turned off to make S_5 turned off. Similarly S_{6a} and S_{6b} are turned off to make S_6 turned off in any case.

The switching pattern of the MOSFETs given in Fig. 2 can be given in Fig. 3. In Fig. 3, T_S, t_{on} and t_{off} represent the switching period, on period and off period of the S_5 switch, respectively. t_{on} is derived by the duty ratio (d) of S_5 determined by the inverter control system, where t_{on} equals to $d \cdot T_S$. The detailed operation procedure of the proposed inverter topology shown in Fig. 2 can be given through Fig. 3 for one sine wave production cycle stage by stage as below. It is clear that each operation stage cycle repeats for each sine wave production cycle given in Fig. 3.

Stage 1 ($0 \leq wt < \pi$)*:* In this stage, the requested sine wave output voltage defined by the reference voltage V_o seen in Fig. 3 is positive. At $wt = 0$, S_2 and S_3 are turned on, S_1 and S_4 are turned off until the end of the stage. S_5 bidirectional switch is controlled through S_{5b} and S_6 bidirectional switch is controlled through S_{6a} in this stage. So, at $wt = 0$, S_{5a} and S_{6b} are turned off until the end of the stage. During this stage, the inverter control system produces time-variant inverter operation duty ratio (d) of S_5 switch for each switching period (T_S). For each T_S, during the on period (t_{on}), S_{5b} is turned on and S_{6a} is turned off. After beginning of the off period (t_{off}), S_{5b} is turned off and S_{6a} is turned on till the end of t_{off}.

Stage 2 ($\pi \leq wt < 2\pi$)*:* In this stage, the requested sine wave output voltage defined by the reference voltage V_o seen in Fig. 3 is negative. At $wt = \pi$, S_1 and S_4 are turned on and S_2 and S_3 are turned off until the end of the stage. S_5 bidirectional switch is controlled through S_{5a} and S_6 bidirectional switch is controlled through S_{6b} in this stage. So, at $wt = \pi$, S_{5b} and S_{6a} are turned off until the end of the stage. During the stage, the inverter control system produces time-variant inverter operation duty ratio (d) of S_5 switch for each switching period (T_S). For each T_S, during the on period (t_{on}), S_{5a} is turned on and S_{6b} is turned off. After beginning of the off period (t_{off}), S_{5a} is turned off and S_{6b} is turned on till the end of t_{off}.

2.3 Snubber circuit design

The snubber circuits are designed for the MOSFETs in Fig. 2 to provide zero-current and zero-voltage switchings to protect them from both the current/voltage stresses and overheating caused by switching losses. The snubber circuits are designed considering the proposed topology, so demonstrating them through the proposed inverter topology is the best way. The proposed inverter circuit with the snubber cells is given in Fig. 4.

As seen from Fig. 4, both series polarised RLD snubber and parallel polarised RCD snubber circuits are designed for each MOSFET active switch. As well known from the literature, the RLD snubber circuit provides zero-current switching during turn on process and the RCD snubber circuit provides zero-voltage switching during turn-off process. So, providing zero-current and zero-voltage switchings prevent occurring of switching losses on the MOSFETs. However, it is clear that switching loss cannot be prevented in the inverter system; just the loss is transferred to the snubber circuit. However, the MOSFETs are prevented from the damage of overheating caused by switching losses. On the other hand, RCD snubber circuits also prevent the MOSFETs from the

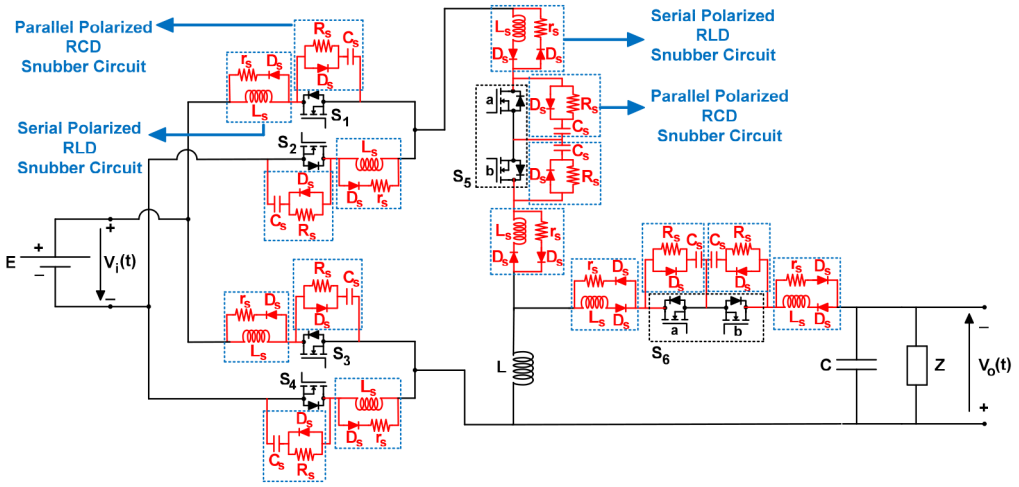

Fig. 4 *Proposed snubber circuits for MOSFETs on the inverter topology*

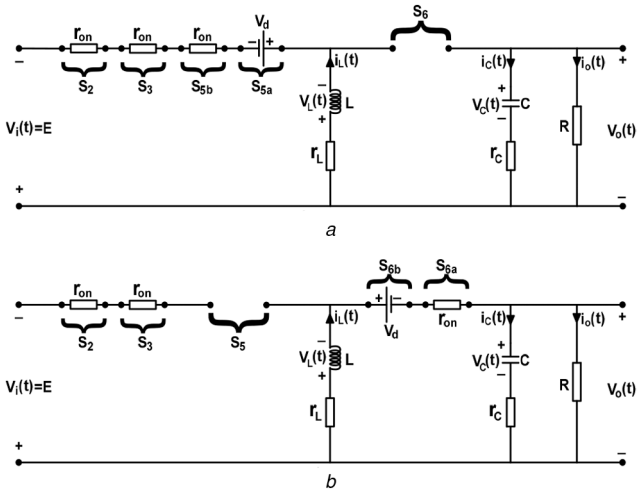

Fig. 5 *Equivalent circuit of the inverter for the case of producing a positive half-wave output voltage*
(a) On mode – S_5 is on, S_6 is off, ***(b)*** Off mode – S_5 is off, S_6 is on

damages of over voltages that have occurred during turn-off process in practical operation, as the current of the leakage inductance of the inverter circuit is forced to be zero.

2.4 Dynamic analysis of the inverter

The dynamic analysis and thus determining the transfer function of the inverter must be done to control the inverter operation. The real parasitic components of both the active switches and the passive elements given in Fig. 2 are considered in the dynamic analysis to be valid and thus efficient in real-time inverter operation. The snubber circuits in Fig. 3 are not considered in the dynamic analysis as they do not affect the inverter operation (in fact negligible). The equivalent circuit during production of positive half-wave sinusoidal voltage at the output of the inverter is given in Fig. 5. In Fig. 1, r_{on}, V_d, r_L, r_C, $V_L(t)$, $i_L(t)$, $V_C(t)$, $i_C(t)$, $i_o(t)$ and R represent on-resistance of the MOSFET, forward biasing voltage of the MOSFET's antiparallel diode, equivalent series resistance (ESR) of the inductor, ESR of the capacitor, inductor voltage, inductor current, capacitor voltage, capacitor current, inverter output current and load resistance, respectively. All of the MOSFETs used in the proposed inverter are selected identical.

The dynamic equations for the case of producing positive half-wave sinusoidal voltage at the output of the inverter can be derived from two operation modes of S_5 switch through the equivalent circuit given in Fig. 5. The target dynamic expressions are the state equations of the inductor current and the output voltage.

Mode 1 (on state) – S_5 is on and S_6 is off: By applying Kirchhoff's Voltage Law (KVL) on the closed loop at the left-hand side of Fig. 5*a*

$$-V_i(t) + (r_L + 3r_{on})i_L(t) + V_d + L\frac{di_L(t)}{dt} = 0 \tag{2}$$

Equation (2) is obtained. The state equation of the inductor current for mode 1 can be derived from (2) as

$$\frac{di_L(t)}{dt} = -\frac{1}{L}(r_L + 3r_{on})i_L(t) + \frac{1}{L}[V_i(t) - V_d] \tag{3}$$

By applying KVL and Kirchhoff's Current Law (KCL) on the closed loop at the right-hand side of Fig. 5*a*

$$\begin{aligned} &V_C(t) + i_C(t)r_C = V_o(t), \\ &i_C(t) = -i_o(t) \\ &\longrightarrow V_C(t) - i_o(t)r_C = V_o(t) \end{aligned} \tag{4}$$

The equation above is obtained. Using (5) given below in (4):

$$i_o(t) = \frac{V_o(t)}{R} \tag{5}$$

state equation of the output voltage for mode 1 can be derived as

$$\frac{dV_o(t)}{dt} = -\frac{1}{RC(1 + (r_C/R))}V_o(t) \tag{6}$$

Mode 2 (off state) – S_5 is off and S_6 is on: By applying KVL on the closed loop at the left-hand side of Fig. 5*b*, the equation below is obtained:

$$L\frac{di_L(t)}{dt} + (r_L + r_{on})i_L(t) + V_d + V_o(t) = 0 \tag{7}$$

The state equation of the inductor current for mode 2 can be derived from (7) as

$$\frac{di_L(t)}{dt} = -\frac{1}{L}(r_L + r_{on})i_L(t) - \frac{1}{L}[V_o(t) + V_d] \tag{8}$$

By applying KVL on the closed loop at the right-hand side of Fig. 5*b* and by applying both KVL and KCL together on the closed loop at the left-hand side of Fig. 5*b*, the equations can be determined as follows:

$$i_L(t) = i_C(t) + i_o(t) \longrightarrow i_C(t) = i_L(t) - i_o(t) \tag{9}$$

$$C\frac{dV_C(t)}{dt} = i_L(t) - \frac{V_o(t)}{R} \tag{10}$$

$$\begin{aligned} V_C(t) + r_C i_C(t) &= V_o(t) \\ &\longrightarrow V_C(t) + r_C[i_L(t) - i_o(t)] = V_o(t) \\ &\longrightarrow V_C(t) + r_C\left[i_L(t) - \frac{V_o(t)}{R}\right] = V_o(t) \end{aligned} \tag{11}$$

Editing (9)–(11) in each other, the state equation of the output voltage for mode 2 can be derived as

$$\begin{aligned} \frac{dV_o(t)}{dt} &= \left(\frac{R}{R+r_C}\right)\left[\frac{1}{C} - \frac{r_C}{L}(r_L + r_{on})\right] i_L(t) \\ &\quad -\left(\frac{R}{R+r_C}\right)\left(\frac{r_C}{L} + \frac{1}{RC}\right) V_o(t) \\ &\quad -\frac{r_C R}{(R+r_C)L} V_d \end{aligned} \tag{12}$$

The state-space equation for on state (mode 1) can be obtained from (3) and (6) as

$$\begin{aligned} \begin{bmatrix} \dot{i_L}(t) \\ \dot{V_o}(t) \end{bmatrix} &= \begin{bmatrix} -\frac{1}{L}(r_L + 3r_{on}) & 0 \\ 0 & -\frac{1}{(R+r_L)C} \end{bmatrix} \begin{bmatrix} i_L(t) \\ V_o(t) \end{bmatrix} \\ &\quad + \begin{bmatrix} \frac{1}{L} & -\frac{1}{L} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_i(t) \\ V_d \end{bmatrix} \end{aligned} \tag{13}$$

The state-space equation for off state (mode 2) can be obtained from (8) and (12) as

$$\begin{aligned} \begin{bmatrix} \dot{i_L}(t) \\ \dot{V_o}(t) \end{bmatrix} &= \begin{bmatrix} -\frac{1}{L}(r_L + r_{on}) & -\frac{1}{L} \\ \frac{R}{R+r_C}\left[\frac{1}{C} - \frac{r_C}{L}(r_L + r_{on})\right] & -\frac{R}{R+r_C}\left(\frac{r_C}{L} + \frac{1}{RC}\right) \end{bmatrix} \begin{bmatrix} i_L(t) \\ V_o(t) \end{bmatrix} \\ &\quad + \begin{bmatrix} 0 & -\frac{1}{L} \\ 0 & -\frac{r_C R}{(R+r_C)L} \end{bmatrix} \begin{bmatrix} V_i(t) \\ V_d \end{bmatrix} \end{aligned} \tag{14}$$

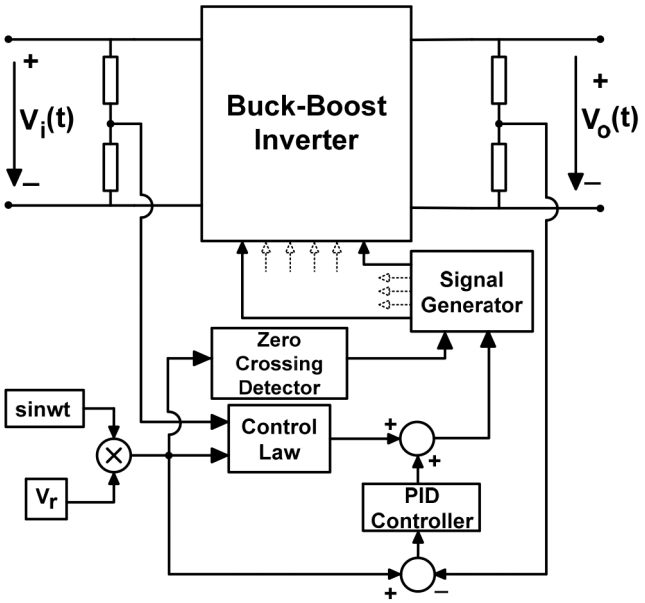

Fig. 6 *General control structure of the inverter*

During the operation case for producing negative half-wave sinusoidal output voltage, the equivalent circuit of the inverter is generally the same in Fig. 5, just differs that S_1, S_4 replace S_2, S_3 and the determined voltages and currents change polarities and directions. So, the state-space equations are valid for the case of producing negative half-wave sinusoidal output voltage.

Using the state-space equations given in (13) and (14), the linearised small-signal transfer function between the inverter output voltage (V_o) and the duty ratio of S_5 (d) is derived as

$$G_S(s) = \frac{\hat{V}_o(s)}{d(s)} = \frac{gs + (ag + cf)}{s^2 + (a+e)s + (ae - bc)} \tag{15}$$

The coefficients given in (15) are described below:

$$a = \frac{(r_L + (1+2\bar{D})r_{on})}{L} \tag{16}$$

$$b = -\frac{(1-\bar{D})}{L} \tag{17}$$

$$c = (1-\bar{D})\frac{R}{R+r_C}\left[\frac{1}{C} - \frac{r_C}{L}(r_L + r_{on})\right] \tag{18}$$

$$e = \frac{\bar{D}}{(R+r_L)C} + (1-\bar{D})\frac{R}{R+r_C}\left(\frac{r_C}{L} + \frac{1}{RC}\right) \tag{19}$$

$$f = -\frac{2r_{on}}{L}\bar{i}_L + \frac{\bar{V}_o}{L} + \frac{V_i(t)}{L} \tag{20}$$

$$\begin{aligned} g &= -\frac{R}{R+r_C}\left[\frac{1}{C} - \frac{r_C}{L}(r_L + r_{on})\right]\bar{i}_L \\ &\quad -\left[\frac{1}{(R+r_C)C} - \frac{R}{(R+r_C)}\left(\frac{r_C}{L} + \frac{1}{RC}\right)\right]\bar{V}_o \\ &\quad + \frac{r_C R}{(R+r_C)L} V_d \end{aligned} \tag{21}$$

In (16)–(21), $\bar{D}$ and $\bar{V}_o$ represent the duty ratio and the output voltage of the inverter at the working point. The relationship between $\bar{D}$ and $\bar{V}_o$ can be given as

$$\bar{V}_o = \frac{\bar{D}V_i}{1-\bar{D}} \tag{22}$$

3 Inverter control through the proposed hybrid control technique

The control of the inverter operation can be given by the general control structure given in Fig. 6.

In Fig. 6, V_r represents the reference peak value of the desired inverter sinusoidal output voltage and this value can be either smaller/higher than or equal to the inverter input voltage V_i. So, the reference sine wave that represents the desired sinusoidal output voltage can be defined as

$$V_{ref}(wt) = V_r \sin wt \tag{23}$$

In (23), w defines the angular frequency of the reference voltage that determines the target frequency of the desired output voltage. Thus, both the desired peak value and the desired frequency of the output voltage are determined through reference voltage equation given by (23).

The signal generator produces the control signal of the inverter active switches S_1, S_2, S_3, S_4, S_5 and S_6.

The zero-crossing detector determines the alternation of the reference sine wave. If the zero-crossing detector determines the reference voltage as positive, the signal generator turns on S_2, S_3 switches and turns off S_1, S_4. Similarly, when the zero-crossing

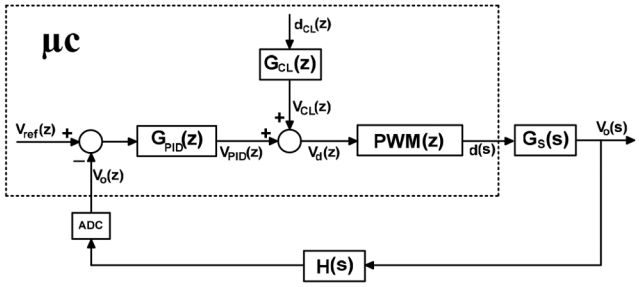

Fig. 7 *Discrete-time control block diagram of the proposed hybrid control technique*

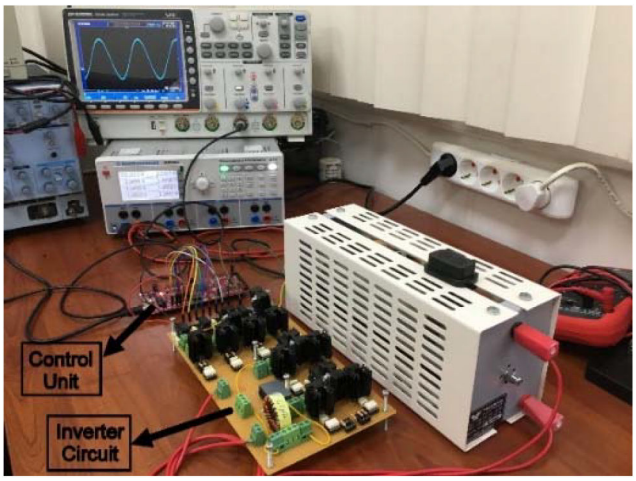

Fig. 8 *Experimental laboratory setup for the proposed single-phase inverter based on buck–boost converter*

detector determines the reference voltage as negative, the signal generator turns on S_1, S_4 switches and turns off S_2, S_3.

The feedback control of the inverter is provided by a proposed hybrid control technique. As seen from Fig. 6, the inverter duty ratio of S_5 (d) is controlled through the traditional PID feedback controller and the proposed open-loop control technique called as CL that supports the feedback PID controller. The PID controller provides elimination of the error between the reference and the real output voltages of the inverter. So the desired output voltage can be obtained with the target response performance through determining the proper controller parameters. However, as it is well known, the controller parameters of PID are determined for a certain system parameter set. So, the determined controller parameters can only provide the desired response performance and also the stability for only the chosen mathematical model of the determined working point. Thus, if the inverter is forced to operate in a different working point, the mathematical model is changed and the determined PID controller parameters cannot meet the desired response performance and may lead the inverter to instability. To provide robust and efficient operation for the proposed inverter with different input and output system parameters, open-loop CL technique is proposed in this paper. In principle, CL determines the open-loop duty ratio of the inverter operation under the assumption that the inverter model is ideal and operates in continuous conduction mode (CCM). From the well known equation of buck–boost converter in ideal and CCM conditions, CL that defines the open-loop duty ratio can be derived as

$$d_{CL}(wt) = \frac{|V_r \sin wt|}{V_i(wt) + |V_r \sin wt|} \tag{24}$$

In practise, the proposed buck–boost-based inverter is not ideal and may also operate in discontinuous conduction mode. So it is clear that only the CL duty ratio cannot meet the required duty ratio of the inverter operation. However, CL duty ratio can support the PID feedback controller to improve the system response performance and stability indirectly when the inverter mathematical model changes. CL produces an inverter duty ratio near the required operation duty ratio in a fast manner by the help of instantaneous static behaviour as seen from (24).

So, the required inverter duty ratio is obtained by the proposed hybrid control system as seen from the mentioned explanations above and Fig. 6

$$d(wt) = d_{CL}(wt) + d_{PID}(wt) \tag{25}$$

Thus, the desired inverter output voltage can be produced in a robust and efficient manner. In the real-time application of the inverter, discrete-time control technique is used through a microcontroller (µc). So, the PID controller, CL and the other control parts given in Fig. 6 are designed in discrete time. The discrete-time block diagram of the proposed hybrid control system that determines the operation duty cycle (d) depending on the structure seen in Fig. 6 can be given in Fig. 7.

In Fig. 7, $V_{ref}(z)$ represents the discrete series of the reference sine wave in (23) and it is produced by the µc.

The real inverter output voltage is discretised through the measurement transfer function $H(s)$ by the analogue-to-digital converter (ADC) embedded in the µc as $V_o(z)$. The discrete open-loop CL duty ratio $d_{CL}(z)$ is produced in the µc directly through (24). $G_{KK}(z)$ is the CL transfer function and can be given as

$$G_{KK}(z) = \frac{1}{\text{PWM}(z)} \tag{26}$$

In (26), PWM(z) defines the transfer function of the PWM process in the µc that determines the inverter operation duty ratio d. In Fig. 7, $G_{PID}(z)$ represents the transfer function of the discrete PID controller. The sum of the discrete PID controller's output signal [$V_{PID}(z)$] and the CL signal [$V_{CL}(z)$] determines the total control signal of the inverter operation duty ratio

$$V_d(z) = V_{PID}(z) + V_{CL}(z) \tag{27}$$

The required inverter operation duty ratio is obtained through the control signal given in (27) and the transfer function of the PWM process as

$$d(s) = \text{PWM}(z) \,.\, V_d(z) \tag{28}$$

4 Real-time application and the results

An experimental setup design and test studies are done for the proposed single-phase inverter based on buck–boost converter to prove its accuracy and efficiency for real-time applications depending on the theoretical analysis given in the previous sections.

4.1 Experimental setup design

The designed experimental laboratory setup for the proposed inverter is shown in Fig. 8. In Fig. 8, the setup is comprised of two main parts: the hardware implementation of the inverter topology and the control unit.

The hardware inverter circuit includes the proposed inverter topology including the main circuit with the snubber cells given in Fig. 4, the driver circuits of the MOSFETs and the auxiliary measurement circuits. The inverter circuit is designed with the values of 0.5 kW, 0–100 V_p and 0–50 Hz. The design criterion limitations are 0–100 V for input direct voltage and 1–100 Ω for output load. Considering the mentioned criterions, IRFP250N-type n-channel, high-speed, low on-resistance MOSFETs (V_{DSS} = 200 V, r_{on} = 75 mΩ and I_D = 30 A) are chosen for the inverter setup circuit for both meeting the current/voltage requirements and the safety margin.

The inductor, the capacitor and the switching frequency (f_S) values of the inverter are determined together through analysing the time constant of the inverter. As the minimum output load is 100 Ω, the time constant is the highest at this load value. On the

Table 1 Determined inductance, capacitance and switching frequency parameters for the experimental inverter circuit

Inductor		Capacitor		Switching frequency f_S, kHz
L, μH	r_L, mΩ	C, nF	r_C, mΩ	
47	100	100	200	10

Table 2 Determined snubber circuits parameters

RLD snubber circuit			RCD snubber circuit		
L_S, μH	r_S, mΩ	D_S	C_S, nF	r_S, Ω	D_S
1	200	1N4004	10	100	1N4004

Table 3 Parameters of considered inverter working point

V_i, V	$\bar{D}$	$\bar{V}_o$, V	R, Ω
30	0.5	30	100

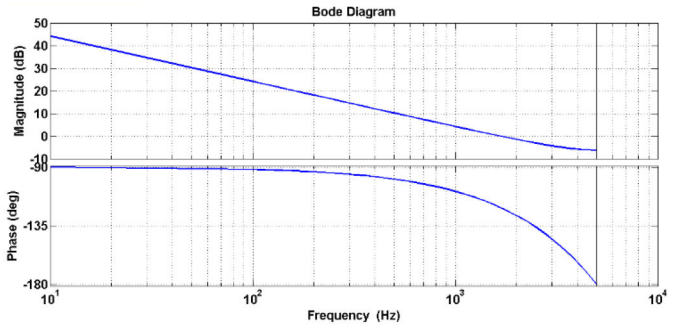

Fig. 9 *Bode diagram of the inverter control block diagram*

other hand, the maximum dv/dt rate of the reference sine wave occurs for 100 V peak value and 50 Hz frequency. So, for the selected f_S value, the rate of the inverter output voltage has to be higher than or equal to the maximum rate of the reference voltage so that the output voltage tracks the reference voltage properly. Depending on the analyses, the determined L, C and f_S values are given in Table 1. In Table 1, the measured ESR values of the selected inductor and the capacitor are also given.

The snubber circuit parameters are determined as given in Table 2. As the MOSFETs are selected identically as mentioned before, the determined parameters in Table 2 are the same for the snubber circuits.

As seen from Fig. 8, the control unit is LAUNCHXL-F28379D microcontroller development kit that includes TMS320F28379D microcontroller core. The microcontroller-based control unit performs producing reference voltage, zero-crossing detection, open-loop CL, discrete PID controller and signal generation processes.

4.2 Discrete PID controller design

The discrete PID controller parameters are determined through the control block diagram given in Fig. 7. In the design of PID controller, $d_{CL}(z)$ is considered zero assuming it as a disturbance. The parameters at the considered inverter working point are given in Table 3.

Considering the parameters given in Tables 1–3 and using (15), the inverter transfer function is derived as

$$G_S(s) = \frac{-5.855 \times 10^6\,\mathrm{s} + 6.125 \times 10^{12}}{s^2 + 1.253 \times 10^5\,\mathrm{s} + 5.546 \times 10^{10}} \tag{29}$$

In Fig. 7, measurement transfer function $H(s) = 1/20$, ADC transfer function equals to 1 and the microcontroller PWM process transfer function equals to 2. Thus, the open-loop transfer function, except PID controller transfer function is determined as below:

$$G(s) = \frac{-5.855 \times 10^5\, s + 6.125 \times 10^{11}}{s^2 + 1.253 \times 10^5\, s + 5.546 \times 10^{10}} \tag{30}$$

The discretised transfer function of $G(s)$ for the sampling period ($T_s = 1/f_s = 1/10\,\mathrm{kHz} = 100\,\mu\mathrm{s}$) can be obtained as

$$G(z) = \frac{11.07\, z + 0.008998}{z^2 + 0.002882\, z + 3.606 \times 10^{-6}} \tag{31}$$

The desired discrete PID controller transfer function can be defined in general form as

$$G_{PID}(z) = K_P + K_I \frac{z}{z-1} + K_D \frac{z-1}{z} \tag{32}$$

where K_P, K_I and K_D represent the well known PID parameters. These parameters are determined through MATLAB–SISOTOOL considering the settling-time and overshoot values as follows:

$$K_P = -1.8 \times 10^{-3}, \quad K_I = 0.0918, \quad K_D = 18 \times 10^{-6} \tag{33}$$

The open-loop inverter transfer function can be obtained using (31)–(33) as below:

$$T(z) = G(z)\,.\,G_{PID}(z) = \frac{0.9963\, z^3 + 0.02033\, z^2 + 0.0002151\, z + 1.62 \times 10^{-7}}{z^4 - 0.9971\, z^3 - 0.002879\, z^2 - 3.606 \times 10^{-6}\, z} \tag{34}$$

The Bode diagram of the inverter's control block diagram given in Fig. 7 through (34) is shown in Fig. 9. In the Bode diagram seen in Fig. 9, the gain margin and the phase margin of the system with the PID controller (except the CL) are obtained as 6.2 dB and 58.96°, respectively.

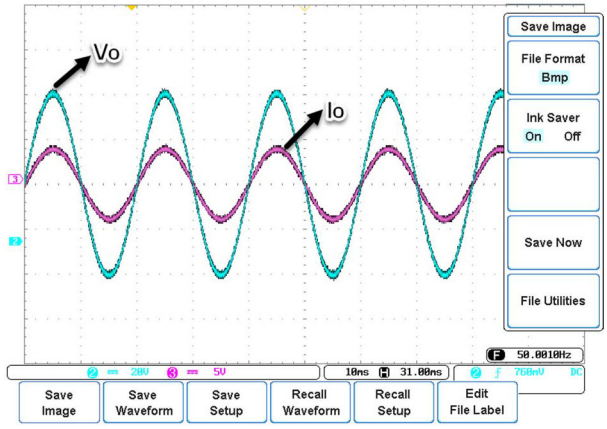

Fig. 10 *Experimental results for case-1 (V/div = A/div for I_o)*

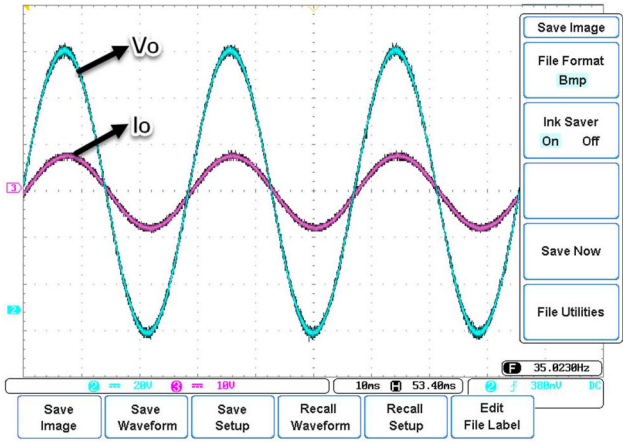

Fig. 11 *Experimental results for case-2 (V/div = A/div for I_o)*

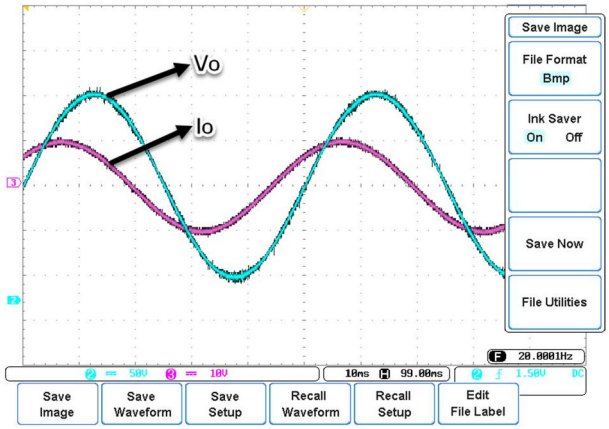

Fig. 12 *Experimental results for case-3 (V/div = A/div for I_o)*

4.3 Experimental results

The proposed single-phase buck–boost inverter has been tested on different input and output conditions through the implemented laboratory setup. The output voltage and current waveforms are obtained from the oscilloscope. These waveforms are transferred to MATLAB to make the THD analyses.

Test case-1: In case-1, inverter input voltage is adjusted as $V_i = 50\,V$. The load is pure resistive and determined as $R = 10\,\Omega$. The desired sine wave output voltage's peak value is $Vo_m = 40\,V$ smaller than the input voltage amplitude and frequency is $f = 50\,Hz$. The output voltage and current waveforms for case-1 are demonstrated in Fig. 10.

As seen from Fig. 10, the desired output voltage is produced close to ideal sine wave with the requested amplitude and frequency. The total output voltage harmonic distortion is measured as $THD_V = \%2.671$. Since the load is resistive, nearly no phase difference has occurred between the inverter output voltage and output current. The total output current harmonic distortion is measured as $THD_I = \%2.643$. Although it is expected that $THD_V = THD_I$ in ideal, THD_I is close to but a little smaller than THD_V as seen from the given experimental results. It is clear that this reason is because of the filtering effect of the leakage inductance of both the load and the circuit paths on the high-order current harmonics.

Test case-2: In case-2, inverter input voltage is adjusted as $V_i = 60\,V$. An inductive load comprised of series-connected resistor and inductor is connected to the inverter output. The resistance and inductance value of the load are $R = 8\,\Omega$ and $L = 5\,mH$, respectively. The desired sine wave output voltage's peak value is $Vo_m = 60\,V$ equal to the input voltage amplitude and frequency is $f = 35\,Hz$. The output voltage and current waveforms for case-2 are given in Fig. 11.

As shown in Fig. 11, the desired output voltage is obtained nearly ideal sine wave with the desired amplitude and frequency. The total output voltage harmonic distortion is measured as $THD_V = \%1.785$. The phase of the output current has lagged according to the output voltage phase because the load is inductive. The total output current harmonic distortion is measured as $THD_I = \%0.434$. As the load is inductive, load inductance filters the high-order harmonics of the output current. So, THD_I is smaller than THD_V.

Test case-3: In case-3, inverter input voltage is selected as $V_i = 40\,V$. A capacitive load comprised of series-connected resistor and capacitor is connected to the inverter output. The resistance and capacitance values of the load are $R = 6\,\Omega$ and $C = 1\,mF$, respectively. The desired sine wave output voltage's peak value is $Vo_m = 100\,V$ higher than the input voltage amplitude and frequency is $f = 20\,Hz$. The output voltage and current waveforms for case-3 are given in Fig. 12. As seen in Fig. 12, the desired output voltage is obtained close to ideal sine wave with the desired amplitude and frequency. The total output voltage harmonic distortion is measured as $THD_V = \%1.063$. The phase of the output current leads the output voltage phase because of the capacitive feature of the load. The total output current harmonic distortion is measured as $THD_I = \%1.732$. The capacitance of the load provides low reactance for the high-order current harmonics. So, THD_I is higher than THD_V for case-3.

Six more test cases are applied to the implemented laboratory setup. The obtained inverter output voltage waveforms and also the output current waveforms are close to ideal sine waveform with the desired amplitude and frequency same as the previous three test cases. The numerical experimental results of the other six test cases are given in Table 4. In Table 4, the inductive and the capacitive loads are series connected. The all experimental results prove that the proposed single-phase buck–boost inverter can produce quality alternative voltages in a wide range that smaller or higher than the inverter input voltage and close to sine form with low THD values with desired frequency. The results also show that the proposed inverter can operate robustly and efficiently on different input and output system conditions. On the different test conditions, the voltage THD values of the output voltage are <5% determined by IEEE standards [41].

In Table 5, the comparative THD results of the output voltages for the proposed buck–boost converter-based single-phase inverter and the similar inverter studies are given together. As seen from Table 5, the proposed inverter has the superiority of providing high-quality output voltage with lower THD values meeting <5% (IEEE standards) in a wide operation range according to the existing buck–boost-based inverter studies in the literature.

Simulation studies in MATLAB–Simulink are also done to show the accuracy and robustness of the proposed inverter study. The comparative output voltage THD values of the simulation results and the experimental results for the test cases 4–9 mentioned before are given together in Table 6. As seen in Table 6, the results of both the simulation and experimental studies are close to each other acceptably.

Table 4 Numerical experimental results for cases 4–9

Test case number	V_i, V	Output load	Desired V_o, V	Desired f, Hz	Obtained V_o, V	Obtained f, Hz	THD_V, %	THD_I, %
4	50	inductive $R = 5\,\Omega$, $L = 1$ mH	35	40	35.02	40.0805	2.989	0.559
5	50	capacitive $R = 5\,\Omega$, $C = 1$ mF	30	30	30.1	30.0293	3.422	4.972
6	60	resistive $R = 20\,\Omega$	60	25	59.96	25.0286	1.756	1.739
7	60	capacitive $R = 5\,\Omega$, $C = 0.5$ mF	60	45	60.07	44.9947	1.818	3.061
8	40	resistive $R = 8\,\Omega$	70	30	70.05	30.0047	1.549	1.522
9	40	inductive $R = 10\,\Omega$, $L = 0.5$ mH	85	50	85.95	50.0061	1.915	0.666

Table 5 Comparative output voltage THD results of the proposed inverter and the similar studies

Study	Output voltage THD, %		
	Best	Worst	Single operating point[a]
proposed inverter	1.063	3.422	—
[20]	2.7	4.1	—
[29]	3	3.7	—
[17]	—	—	4.6
[34]	—	—	8.85

[a]Indicates that the study is done for only one operating point.

Table 6 Comparative output voltage THD values of the simulation and experimental studies

Study type	Output voltage THD, %					
	Test case-4	Test case-5	Test case-6	Test case-7	Test case-8	Test case-9
sim.	2.095	2.398	1.231	1.274	1.086	1.342
exp.	2.989	3.422	1.756	1.818	1.549	1.915

sim. = simulation and exp. = experimental.

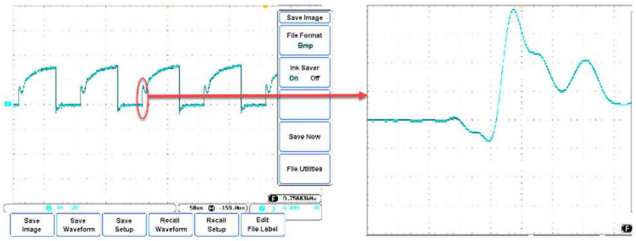

Fig. 13 *Drain–source current I_{DS} waveform of S_{5a} MOSFET for case-8 during on switching (V/div = A/div for I_o)*

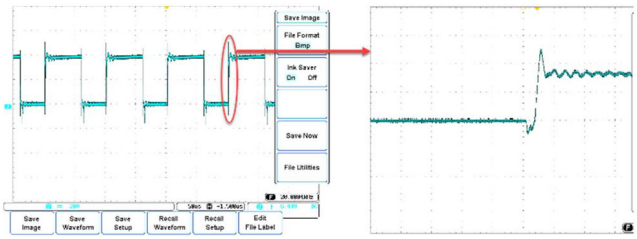

Fig. 14 *Drain–source voltage V_{DS} waveform of S_{5a} MOSFET for case-8 during off switching (RCD snubber circuit exists)*

The desired effects of the proposed snubber circuits are demonstrated in Figs. 13–15.

Fig. 13 demonstrates the effect of RLD snubber circuit for S_{5a} MOSFET on the drain–source current during on switching for the test case-8. As seen in Fig. 13, the RLD snubber circuit provides zero-current switchings reducing the di/dt rate of the drain–source current.

Figs. 14 and 15 show the drain–source voltage waveforms of S_{5a} MOSFET during off switching in the case of the RCD snubber circuit exists or not for the test case-8.

As seen from Figs. 14 and 15, the RCD snubber circuit provides zero-voltage switching reducing the dv/dt rate of the drain–source voltage and prevents occurring overvoltage.

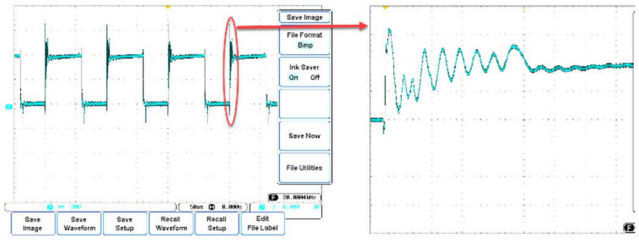

Fig. 15 *Drain–source voltage V_{DS} waveform of S_{5a} MOSFET for case-8 during off switching (RCD snubber circuit does not exist)*

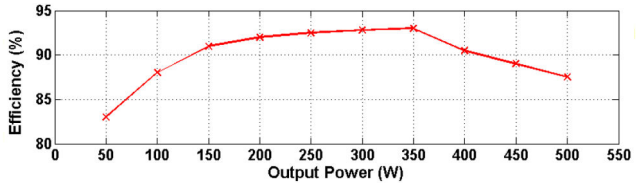

Fig. 16 *Efficiency curve of the proposed inverter*

The efficiency analysis of the proposed inverter is done for different power levels at the operating point of $V_i = 30$ V and $Vo_m = 80$ V. The obtained efficiency curve is shown in Fig. 16.

As seen in Fig. 16, the efficiency of the proposed inverter increases until nearly 70% of the maximum that is 350 W. After increasing the power level than 350 W, the efficiency decreases. Even so, the average efficiency of the proposed inverter is well about 90%.

5 Conclusion

In this paper, a single-phase buck–boost inverter with reduced number of components is presented. The proposed inverter topology has a novel structure including snubber circuits providing zero-voltage/current switching and reducing-voltage/current stresses. Unlike the similar studies in the literature, a novel hybrid control technique comprised of the traditional feedback PID controller and the newly designed open-loop CL control method is

applied to the proposed inverter to achieve robust and efficient operation under different working conditions. An experimental laboratory setup with the values of 0.5 kW, 0–100 V_p and 0–50 Hz is implemented for the real-time inverter operation. The experimental results show that the proposed inverter has the ability of producing alternative voltage close to ideal sine waveform with low THD values under 5% on different inverter operation conditions in a wide range through bucking and boosting structures.

6 Acknowledgments

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